T-Engine Expansion Board Design Guidelines

Ver. 1.00.01

TEF010-S008-01.00.01/en

June 2009

T-Engine Forum

http://www.t-engine.org/

CONTENTS

■ Chapter 1 Introduction

1.1. About this document

These Design Guidelines describe, for system developers developing systems by expanding hardware based on T-Engine, design guidelines for expansion boards connected via the external expansion bus connectors of standard T-Engine and μT-Engine.

Chapter 2 describes the physical specifications of expansion bus connectors, keying and other shared areas, and classification of T-Engine expansion bus signal assignments.

Chapters 3 and later describe the design method for the expansion bus used in each T-Engine product.

■ Chapter 2 T-Engine hardware

2.1. Summary of T-Engine hardware

Through strong standardization of the real-time operating system for embedded systems, T-Kernel, the T-Engine Forum has sought to improve the efficiency of developing embedded systems by making the distribution of middleware possible. It has standardized both standard T-Engine and μT-Engine as standard development platforms for embedded systems using T-Kernel, leading to the commercialization of a large number of products using CPU cores with high market shares worldwide, such as ARM and MIPS. These include products using Japanese CPU cores such as SH, M32R, and FR.

Both standard T-Engine and μT-Engine feature expansion bus connectors for hardware expansion purposes. These make it possible to build any number of systems by connecting expansion boards to these connectors.

Basically, the CPU bus outputs to the T-Engine expansion bus connector. The T-Engine standards do not specify signal assignments for the expansion bus connectors. This is because CPU buses vary by manufacturer and model, and reliance on a single bus standard could restrict the performance of products using other bus protocols or cause the standard to become outdated if it were incompatible with CPUs using new architectures were to be introduced in the future. Assignment of signals optimized for each model makes it possible to demonstrate to the fullest the performance of the CPU used.

Standard T-Engine and μT-Engine are hardware serving as development platforms for running T-Kernel. A development platform is a computer system used as a prototype when developing an embedded system.

Standard T-Engine employs a 32-bit CPU and requires a memory management unit (MMU). It features user interfaces such as LCD displays with touch panels, buttons, and voice input/output. It also supports a wealth of general-purpose interfaces such as PC Card and USB host functions for hardware expansion purposes or for connecting flash memory and other media for storing programs. Despite its high level of performance, standard T-Engine is very compact. With a battery attached, it could be used as a prototype for a PDA.

On the other hand, μT-Engine does not require any user interface such as a screen or voice input or output. As a result, it is even more compact in size. It also uses a 32-bit CPU as standard, but it does not require an MMU. As an external interface, it uses a Compact Flash interface and an MMC or SD card slot, which are even smaller in size than the interfaces used by standard T-Engine. It uses more than one type of memory-card interface so that when one is used as media for storing programs the other can be used as an interface for hardware expansion using peripherals.

Although standard T-Engine and μT-Engine differ in terms of the interfaces they feature and of external dimensions, they employ an identical architecture and both run T-Kernel.

Figures 2.1.1 and 2.1.2 show examples of standard T-Engine and μT-Engine board structures, and Figure 2.1.3 shows an example CPU board structure. The CPU board includes all basic functions for running the system, such as the CPU, memory, and power circuitry. As such, a CPU board could run on its own. Functions can be expanded around a CPU board by combining it with an LCD board, an expansion board, and a debugging board. μT-Engine

does not require an interface with an LCD board. With an expansion bus connector plug and receptacle on either side of each expansion board, multiple boards can be stacked and used together.

The T-Engine Forum has standardized the external dimensions of these boards and the positions of external interface connectors on them. As such, the same housing can be used even for different CPUs.

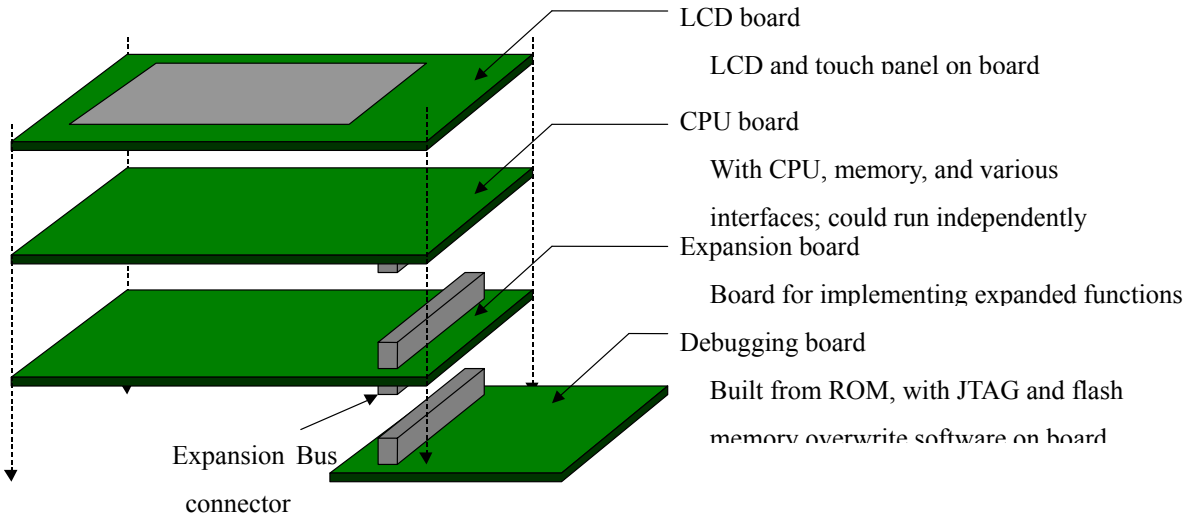


Figure 2.1.1: Standard T-Engine system structure example

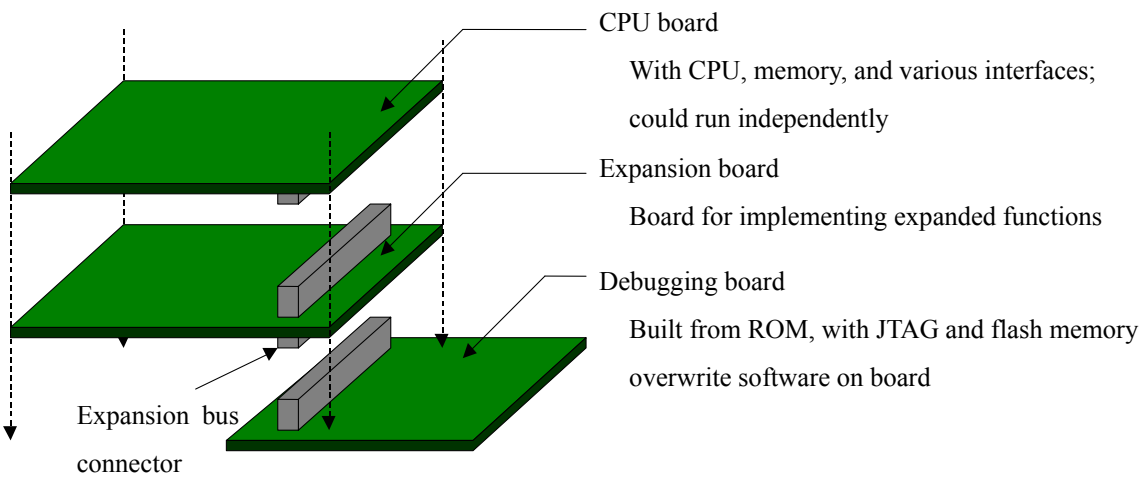


Figure 2.1.2: μT-Engine system structure example

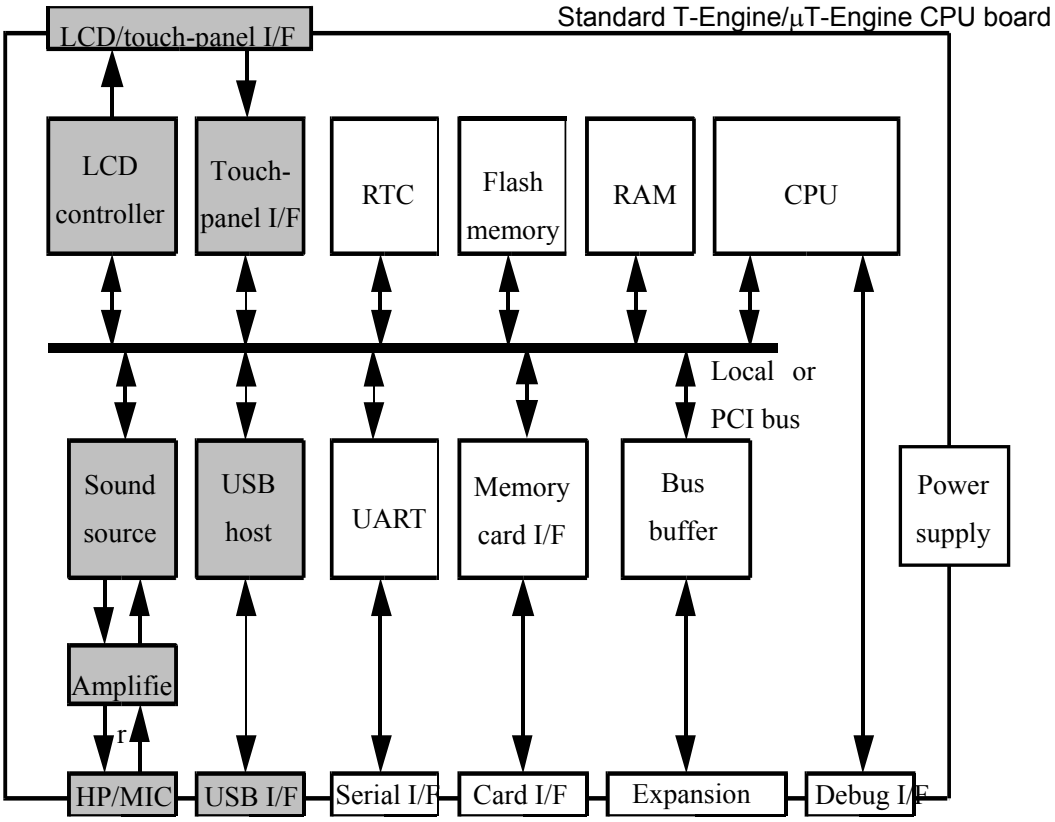


Figure 2.1.3: Standard T-Engine/μT-Engine standard CPU board structure example

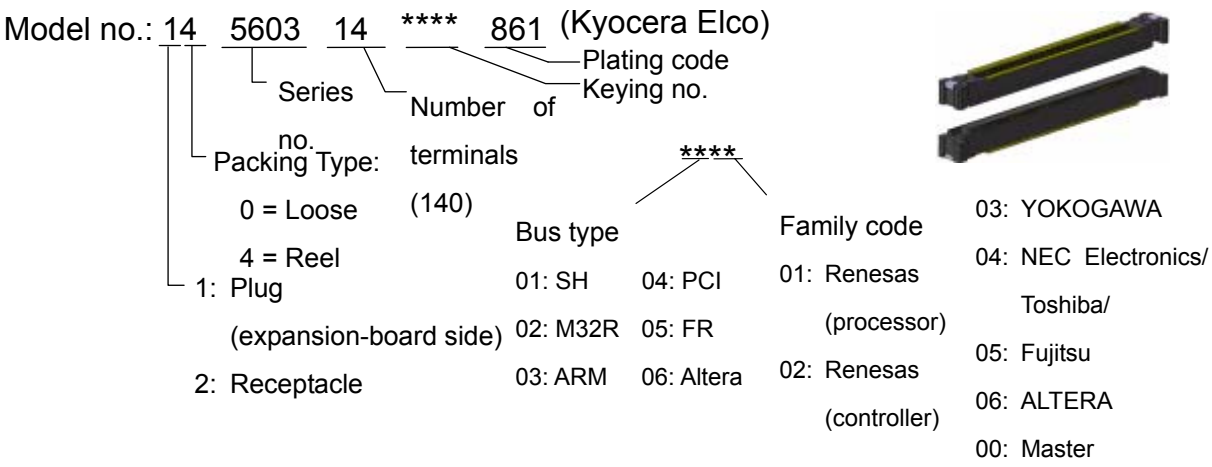
2.2. T-Engine expansion bus connectors

As described above, the T-Engine standard does not specify expansion bus connector signal assignment. To prevent damage to a T-Engine unit or to an expansion board by inserting an expansion board built for a different T-Engine, keys are attached to both sides of the expansion bus connector to prevent incorrect insertion. These keys are assigned by the T-Engine Forum based on the type of bus output to the expansion bus connector.

Figure 2.2.1 shows T-Engine keying as currently assigned. On one side, KEY-A indicates the bus type, while on the other side KEY-B indicates the family code. The keying of "00" is the master key. For example, boards such as a power supply board and an FPGA board, which can be used without regard to differences in buses, use the master key, which means they can be connected to any T-Engine.

In some T-Engine products, both a local bus and a PCI bus output to the expansion bus connector. The PCI bus is a standard for connecting a CPU and peripheral devices on a circuit board. Signal assignment for the PCI bus on a T-Engine expansion bus connector that has a PCI bus is standardized (bus type 04), so that an expansion board with a PCI bus can be used with any T-Engine product that has a PCI bus.

Developed for PCs and workstations, there is a large number of diverse devices on the market that use PCI buses, such as networking and graphics devices. As such, users can enjoy a wide choice of components for PCI buses.



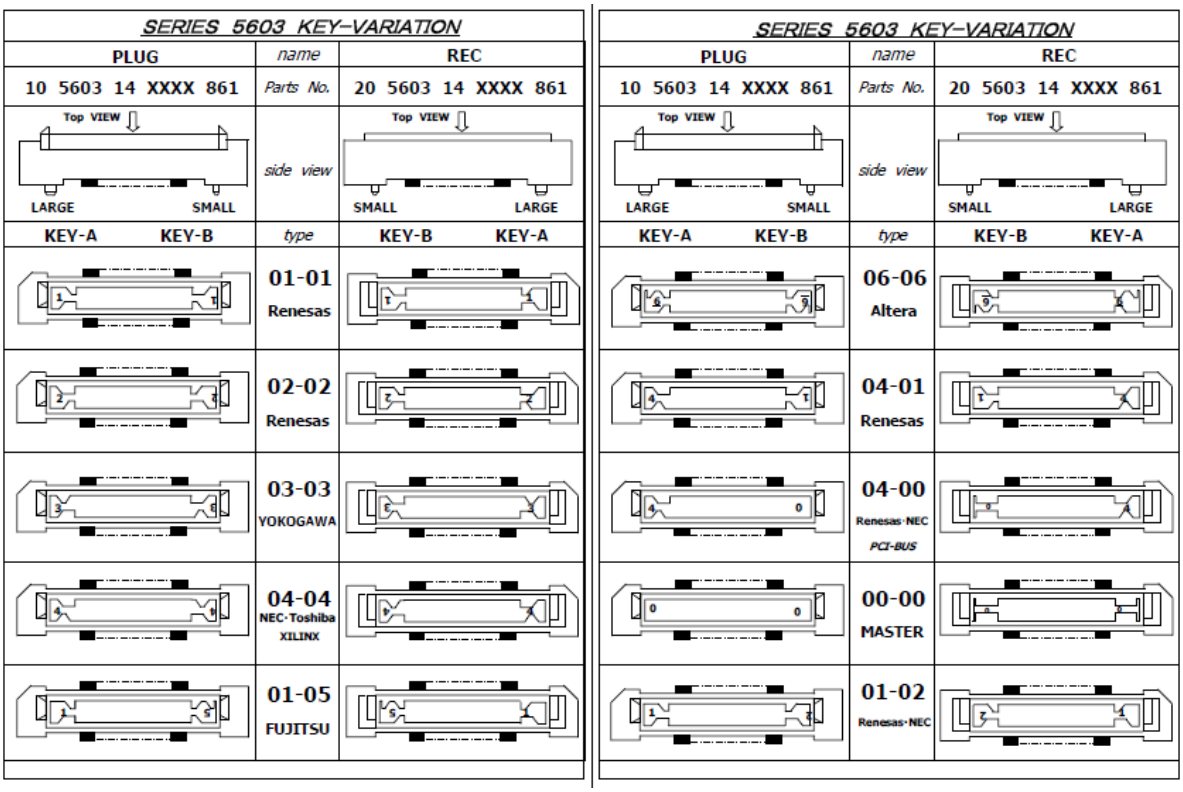


Figure 4.1.1: Keying allocation to prevent incorrect insertion of expansion bus connector.

2.3. Categories of T-Engine expansion buses

Expansion buses are categorized into several groups. Table 2.3 lists expansion bus connector signal-assignment groups by product. The biggest difference is that between connectors to which only the local bus is output and those to which the PCI bus is also output. Among those to which the local bus is output, consideration has been given to matching signal assignments as much as possible.

See Appendix B of T-Engine Design Gide lines concerning specific pin assignments for each T-Engine and μT-Engine product.

Table 2.3: Expansion bus connector signal assignment groups

Architecture family	Group							
	PCI		Local bus					
	SH-4	MIPS	SH-2/V830	M32R	SH-3/SH-4	ARM	FR	Nios
	04-01	04-04	01-02	02-02	01-01	03-03	01-05	06-06
Renesas Technology	SH7751							
					SH7727			
					SH7760			
			SH7145					
				M32104				
				M32192				
NEC Electronics		VR5500						
		VR4131						
			V850E/MA3					
Toshiba Information Systems		TX4956						
Yokogawa Digital Computer						ARM926-MB8		
						ARM922-LH7		
						ARM920-MX1		
						ARM720-LH7		
						ARM720-S1C		
Fujitsu Micro Electoronics							MB91403	
Altima								Nios II

2.4. Hardware development using T-Engine

(1) Hardware expansion using the local bus

A CPU's local bus is an interface intended for connection to devices with addresses mapped to memory or I/O space. The most common device connected to the local bus is memory. For this reason, the T-Engine's CPU can access user circuitry in accordance with memory protocols supported by the CPU.

Since the local bus has a wide bus width and enables use of DMA and interrupts, it is a high performance interface which offers a high level of freedom and with the highest level of freedom. However, note that since local-bus protocols vary by manufacturer and CPU type an expansion board developed for one T-Engine will not necessarily run on another T-Engine.

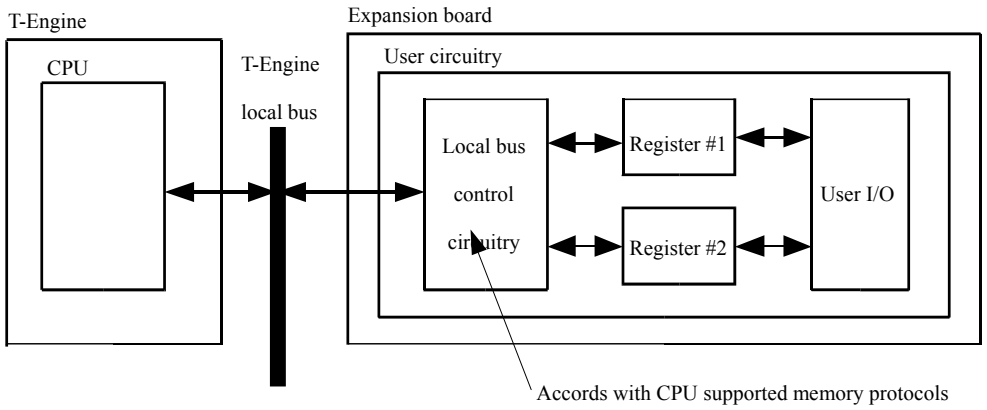


Figure 2.4.1: Structural example of an expansion board using a local bus

(2) Hardware expansion using the PCI bus

The PCI bus is a standard for connecting a CPU with peripheral devices on a circuit board. An appeal of the PCI bus is the wide range of component choices, since it can be used to connect CPUs and peripheral devices regardless of their manufacturers or types and, more than anything else, because of the large and diverse range of PCI devices on the market for PCs and workstations.

The PCI pin assignments for T-Engine expansion bus connectors using PCI buses are standardized. For this reason, a PCI expansion board can be used by any T-Engine with a PCI bus.

Since PCI is a bus structure, mediation is required between bus-master devices connected to a bus. The device that handles this mediation is referred to as the PCI host or the central resource. A T-Engine with a PCI bus also features this PCI host function, making it possible to connect up to three PCI devices.

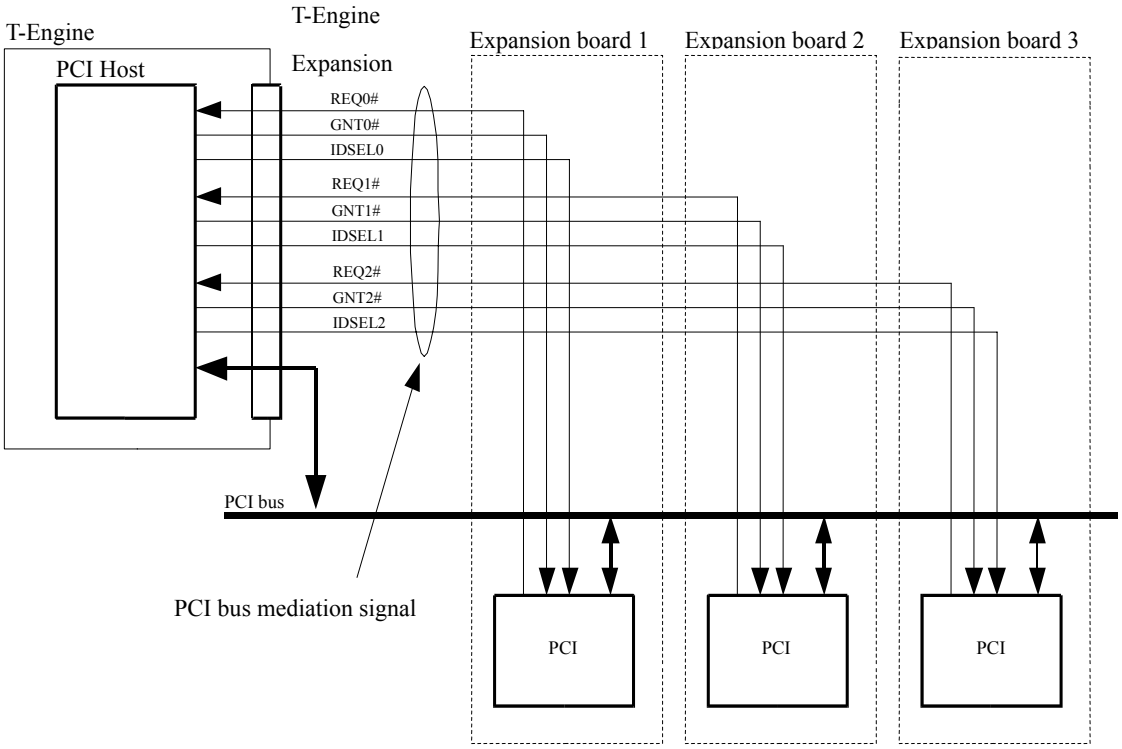


Figure 2.4.2: Structure of an expansion board using a PCI bus

(3) Expansion boards for development purposes

A universal expansion board and an FPGA board are on the market for developing circuitry for connecting to the T-Engine expansion bus connector.

○ Universal expansion board

The universal expansion board draws T-Engine expansion bus connector signals, which are difficult to wire by hand, through 2.54-mm-pitch throughholes, making it easy for users to expand hardware. (See Figure 2.4.3.) The board features a 2.54-mm-pitch universal area, making it possible to connect any circuitry through hand wiring. This board is optimal for connecting relatively small-scale user circuitry, such as sensors and simple I/O devices.

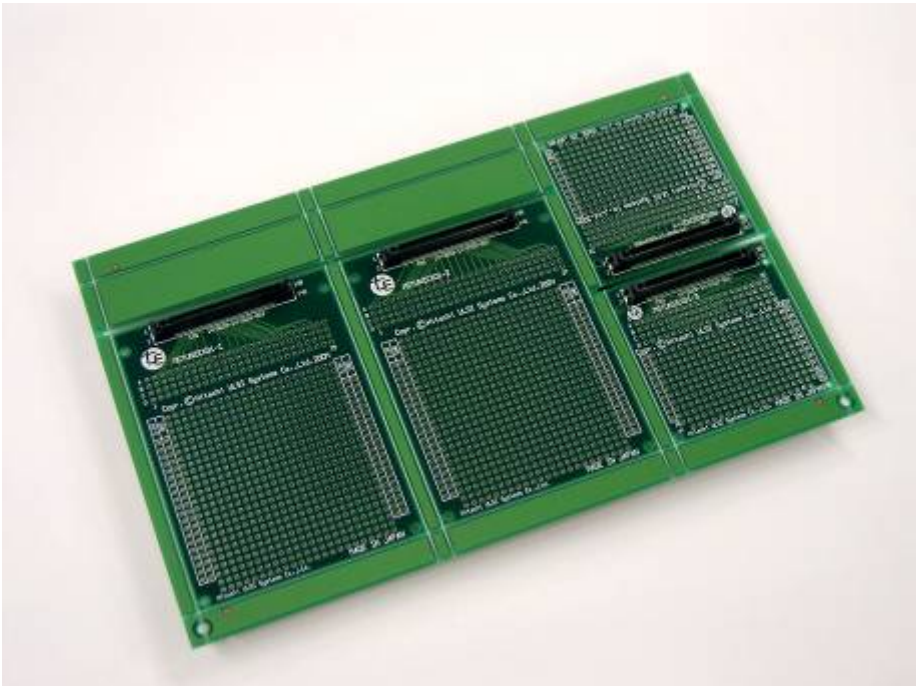


Figure 2.4.3: Universal expansion board

○ FPGA development board for functional expansion (Altima)

The FPGA development board is convenient to use when developing large-scale circuitry for which the universal expansion board is not suited. FPGA stands for “field programmable gate array,” referring to a type of LSI circuit with internal circuitry that can be programmed by the user externally. An FPGA includes a number of logical blocks centered on a flip-flop circuit known as a logic element. These can be programmed externally to create the desired logical circuit.

Figure 2.4.4 shows the structure of an FPGA development board for functional expansion developed for use with T-Engine, and Figure 2.4.5 shows an exterior view of the board.
The FPGA included on the board is Altera’s Cyclone EP1C20, with approximately 20,000 logic elements. Officially, it can be used to build circuits of the scale of approximately 250,000 gates. It also can be used as an ASIC trial environment. In addition, since the board features SDRAM, it is compatible with large-scale systems using high-speed, high-capacity memory.

This FPGA board is compatible with all T-Engine units, because by connecting all terminals of a T-Engine expansion bus connector to the FPGA the latter can be used to compensate for bus protocol differences. Its key for preventing incorrect insertion is a master key usable with all T-Engine units.

Since the internal logic of the FPGA can be modified easily through reprogramming, this board makes it possible to shorten the turnaround time from making design changes through testing actual prototypes. In general, production of LSI devices such as ASIC devices takes a long time: several months. However, using an FPGA as a trial environment makes it possible to debug prototypes while conducting logical design, resulting in dramatic improvements to the efficiency of design and testing.

Since T-Engine units are shipped with the T-Kernel real-time operating system for embedded devices ready to run from the start, the efforts to port an operating system and build a debugging environment usually needed when starting up a hardware development environment are not needed. Furthermore, with hardware development environments such as the universal expansion board and the FPGA board making short turnaround times feasible, hardware development can be conducted at the same time as software development.

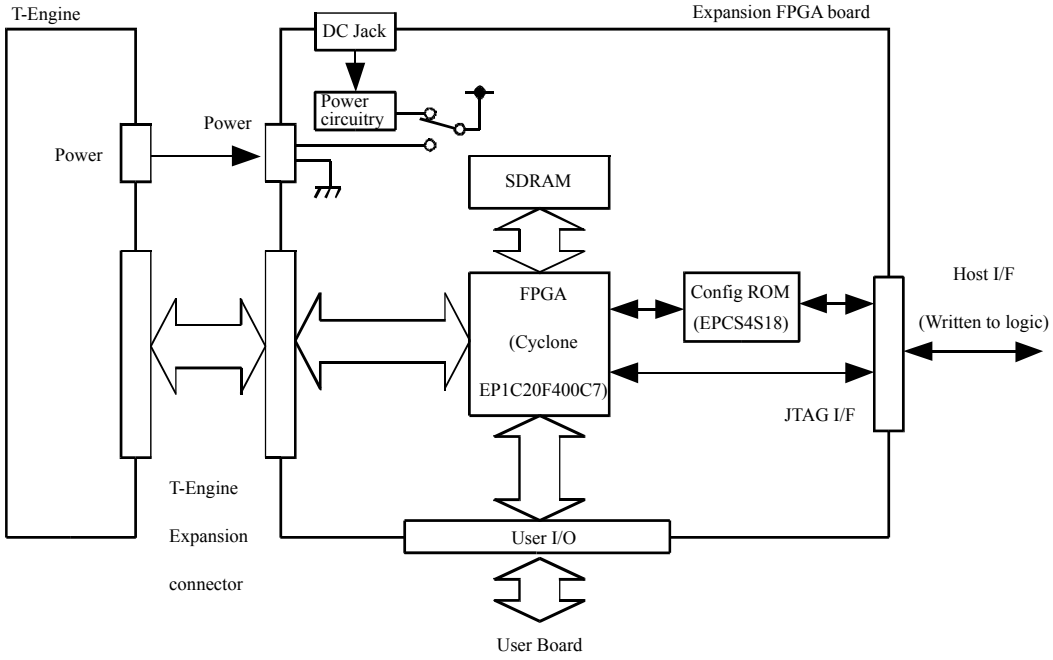


Figure 2.4.4: Structure of Expansion FPGA board manufactured by ALTIMA

Figure 2.4.5: Exterior view of an expansion FPGA board manufactured by ALTIMA

○ Expansion FPGA development board (XILINX)

This expansion board with FPGA manufactured by XILINX, Inc. expands the capability of T-Engine easily. Figure 2.4.6 shows structure of Expansion FPGA board manufactured by XILINX.

FPGA is a logic device, which can be re-programmed many times by users. Being able to re-program the designed circuit quickly makes the device highly effective in improving development efficiency.

FPGA in this board is Spartan-3E XC3S500E (half-million system gates) manufactured by XILINX Corp. Aside from logic cells, it is equipped with block memory of 360KB in total and 20 multipliers of 18X18 bits which are effective in signal processing. In addition, it is possible to mount MicroBlaze, the 32 bit RISC processor manufactured by XILINX Corp. This board can be used as sub-processor in addition to the main T-Engine, and can expand the system function very much.

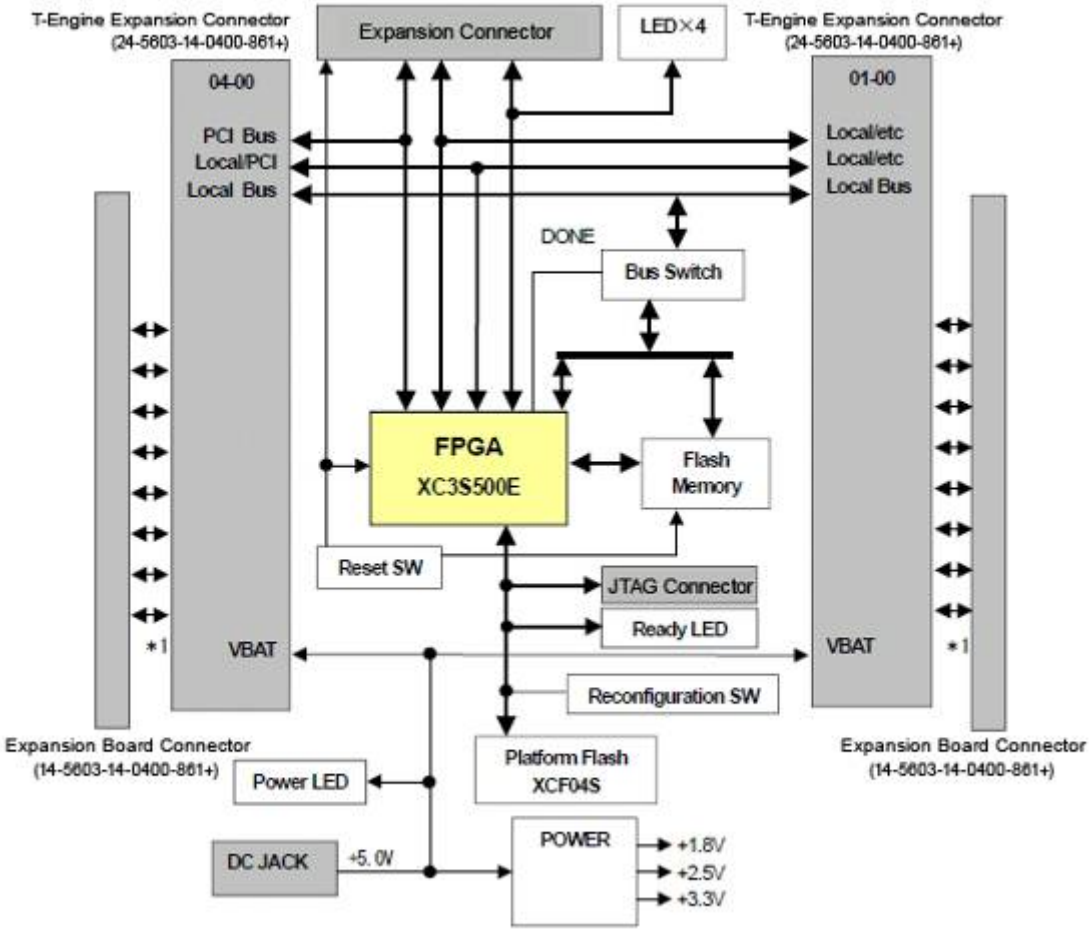


Figure 2.4.6: Structure of Expansion FPGA board manufactured by XILINX

In terms of connection to T-Engine, expansion bus connector keying is devised to prevent an error due to incorrect insertion. Two types of buses, SH system bus 01-00 and PCI system bus 04-00, are equipped as a standard. Therefore, you can connect T-Engine boards with SH system bus and PCI system bus directly and safely.

Regarding the bus for connection to T-Engine with other types of keying, the offered conversion adaptor makes it possible to connect them to all T-Engine/μT-Engine safely according to the specification.

100-pin connector is also equipped for additional expansion.

Substantial improvement of efficiency can be expected by using the expansion FPGA board during development. Besides, T-Engine's possibilities can be expanded significantly by using many capabilities of the mounted FPGA manufactured by XILINX Corp.

■ Chapter 3 SH7727/SH7760 T-Engine expansion board design guidelines

This chapter describes design guidelines for expansion boards connecting via SH7727/SH7760 T-Engine expansion slots.

The expansion board refers to a board featuring user selected devices etc. and controllable using the SH7727/SH7760 address bus, data bus, and control signals or serial (start-stop synchronization) signals output to the T-Engine expansion bus connector.

3.1. SH7727/SH7760 T-Engine expansion bus connector specifications

T-Engine connector type implemented: 20-5603-14-0101-861+ (Kyocera Elco)

Compatible connector type: 10-5603-14-0101-861+ (Kyocera Elco)

Figure 3.1 shows the arrangement of the expansion bus connector.

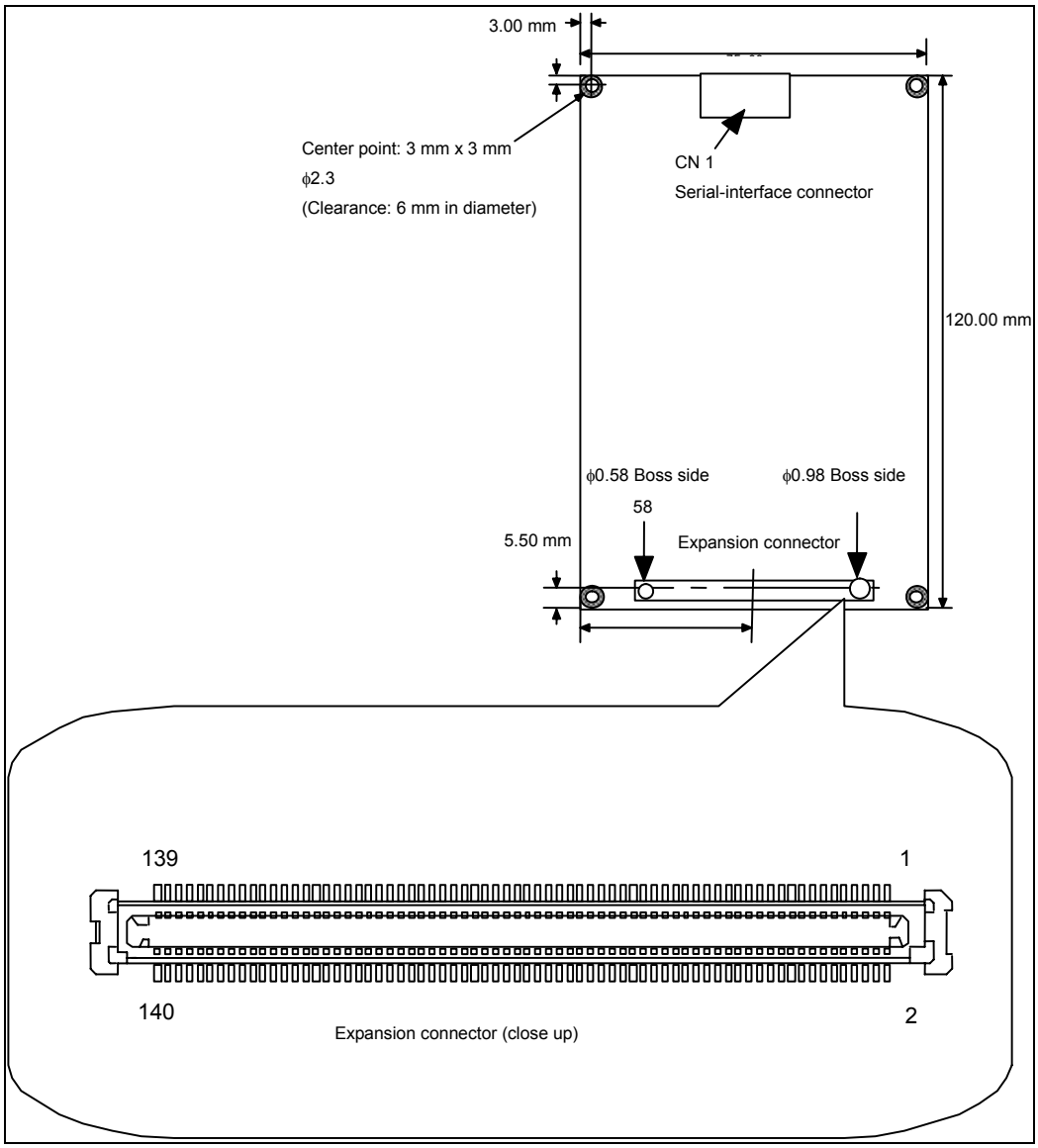


Figure 3.1: Expansion bus connector arrangement

3.2. Expansion bus connector signal arrangement

Table 3.2 shows the arrangement of expansion slot signals.

Table 3.2: Expansion slot signal arrangement

Pin No.	Signal	I/O	Pin No.	Signal	I/O	Pin No.	Signal	I/O	Pin No.	Signal	I/O
1	5V (*1)	-	36	D29	I/O	71	A24	OUT	106	SH7727_CTS2	IN
2	5V	-	37	D30	I/O	72	A25	OUT	107	-	-
3	5V	-	38	D31	I/O	73	~EPROMCE	OUT	108	ASEMD0	IN
4	5V	-	39	GND	-	74	~CS2	OUT	109	GND	-
5	D0	I/O	40	GND	-	75	~CS4	OUT	110	GND	-
6	D1	I/O	41	CKIO	OUT	76	~CS5	OUT	111	TCK	IN
7	D2	I/O	42	GND	-	77	RDWR	OUT	112	TMS	IN
8	D3	I/O	43	GND	-	78	~BS	OUT	113	~TRST	IN
9	D4	I/O	44	GND	-	79	GND	-	114	TDI	IN
10	D5	I/O	45	A0	OUT	80	GND	-	115	TDO	OUT
11	D6	I/O	46	A1	OUT	81	~RD	OUT	116	~ASEBRKAK	OUT
12	D7	I/O	47	A2	OUT	82	~WAIT	IN	117	3.3VSB (*3)	-
13	D8	I/O	48	A3	OUT	83	~WE0	OUT	118	3.3VSB	-
14	D9	I/O	49	A4	OUT	84	~WE1	OUT	119	3.3VSB	-
15	D10	I/O	50	A5	OUT	85	~WE2	OUT	120	3.3VSB	-
16	D11	I/O	51	A6	OUT	86	~WE3	OUT	121	AUDATA0	I/O
17	D12	I/O	52	A7	OUT	87	GND	-	122	AUDATA1	I/O
18	D13	I/O	53	A8	OUT	88	GND	-	123	AUDATA2	I/O
19	D14	I/O	54	A9	OUT	89	~IRQ0	IN	124	AUDATA3	I/O
20	D15	I/O	55	A10	OUT	90	~IRQ1	IN	125	~AUDSYNC	OUT
21	GND	-	56	A11	OUT	91	~IRQ2	IN	126	AUDCK	IN
22	GND	-	57	A12	OUT	92	~IRQ3	IN	127	3.3V (*4) Δ1	-
23	D16	I/O	58	A13	OUT	93	NMI_IN	IN	128	3.3V Δ1	-
24	D17	I/O	59	A14	OUT	94	~RST_IN	IN	129	3.3V Δ1	-
25	D18	I/O	60	A15	OUT	95	~RST_OUT	OUT	130	3.3V Δ1	-
26	D19	I/O	61	GND	-	96	~DREQ0	IN	131	3.3V Δ1	-
27	D20	I/O	62	GND	-	97	~DRAK0	OUT	132	3.3V Δ1	-
28	D21	I/O	63	A16	OUT	98	~DACK0	OUT	133	VBAT_IN (*5) Δ1	-
29	D22	I/O	64	A17	OUT	99	ROMSEL	IN	134	VBAT_IN Δ1	-
30	D23	I/O	65	A18	OUT	100	~BASE (*2)	IN	135	VBAT_IN Δ1	-
31	D24	I/O	66	A19	OUT	101	GND	-	136	VBAT_IN Δ1	-
32	D25	I/O	67	A20	OUT	102	GND	-	137	GND Δ1	-
33	D26	I/O	68	A21	OUT	103	SH7727_TXD2	OUT	138	GND Δ1	-
34	D27	I/O	69	A22	OUT	104	SH7727_RXD2	IN	139	GND Δ1	-
35	D28	I/O	70	A23	OUT	105	SH7727_RTS2	OUT	140	GND Δ1	-

Shaded areas denote SH7727/SH7760 address bus, data bus, control signals, and serial signals. The electrical power level is 3.3 V.

*1: When the SH7727/SH7760 unit's power is on, power of 5.0 V (typ.) is supplied.

*2: By setting this terminal to the low level, the SH7727/SH7760 expansion bus will be output to the expansion slot.

*3: When a battery or an AC adapter is connected, power of 3.3 V (typ.) is supplied at all times.

*4: When the SH7727/SH7760 unit's power is on, power of 3.3 V (typ.) is supplied.

*5: This is the terminal for the power supply from the power supply board (4.2 – 3.7 V). Power can be supplied from the power-supply board to the T-Engine.

3.3. Areas over which the expansion board can be expanded

3.3.1. SH7727 T-Engine memory map

Table 3.3.1 shows the SH7727's memory map.

As shown in Table 3.3.1, the expansion board can be expanded to three areas: Area 2, Area 4, and Area 5.

Since the wait number and bus width for each area can be set by configuring the bus controller inside the SH7727, devices with different access speeds and different bus widths can be used together.

Table 3.3.1: SH7727 memory map

Area No.	Bus width	Space	Space name	Device	Notes
Area 0	16 bit	h'00000000 ~ h'007FFFFF	Flash memory area	8 MB MBM29DL640E90TN (Fujitsu) x 1	
		h'00800000 ~ h'00FFFFFF	-	Flash memory area image	
		h'01000000 ~ h'03FFFFFF	-	Unused area	
Area 1	-	h'04000000 ~ h'07FFFFFF	SH7727 Internal area		
Area 2	8/16/32 bit	h'08000000 ~ h'0BFFFFFF	-	64 MB Expansion-board expansion area 2 Can be used freely by user via expansion bus connector (/CS2)	
Area 3	32 bit	h'0C000000 ~ h'0DFFFFFF	SDRAM area	32 MB HM5225325FBP-B60 (Hitachi) x 1	
		h'0E000000 ~ h'0FFFFFFF	-	Unused area	
Area 4	8/16/32 bit	h'10000000 ~ h'13FFFFFF	-	64 MB Expansion-board expansion area 4 Can be used freely by user via expansion bus connector (/CS4)	
Area 5	8/16/32 bit	h'14000000 ~ h'17FFFFFF	-	64 MB Expansion-board expansion area 5 Can be used freely by user via expansion bus connector (/CS5)	
Area 6	16 bit	h'18000000 ~ h'19FFFFFF	PC CARD area	Card controller Model: MR-SHPC-01 V2T (Marubun) (Referred to as "SH-PCIC" hereinafter)	
		h'1A000000 ~ h'1AFFFFFF	UART area (ChA)	UART Model: ST16C2550CQ48 (EXAR) (Referred to as "UART" hereinafter)	
		h'1B000000 ~ h'1BFFFFFF	UART area (ChB)	Same as above	
Area 7	-	h'1C000000 ~ h'1FFFFFFF	-	-	Reserved

3.3.2. SH7760 T-Engine memory map

Table 3.3.2 shows the SH7760's memory map.

As shown in Table 3.3.2, the expansion board can be expanded to three areas: Area 2, Area 4, and Area 5. Since the wait number and bus width for each area can be set by configuring the bus controller inside the SH7760, devices with different access speeds and different bus widths can be used together.

Table 3.3.2: SH7760 memory map

Area No.	Bus width	Space	Space name	Device	Notes
Area 0	16 bit	h'00000000 ~ h'00FFFFFF	Flash memory area	8 MB MBM29DL640E90TN (Fujitsu) x 1	
		h'01000000 ~ h'03FFFFFF	-	Unused area	
Area 1	16 bit	h'04000000 ~ h' 07FFFFFF	Board control register area	16 MB Board control register	
Area 2	8/16/32 bit	h'08000000 ~ h'0BFFFFFF	Expansion area (CS2)	64 MB Expansion slot (CS2 area)	Expansion slot CS2# assertion
Area 3	32 bit	h'0C000000 ~ h'0FFFFFFF	SDRAM area	64 MB EDS2516APTA-75 (ELPIDA) x 2	
Area 4	8/16/32 bit	h'10000000 ~ h'13FFFFFF	Expansion area (CS4)	64 MB Expansion slot (CS4 area)	Expansion slot CS4# assertion
Area 5	8/16/32 bit	h'14000000 ~ h'17FFFFFF	Expansion area (CS5)	64 MB Expansion slot (CS5 area)	Expansion slot CS5# assertion
Area 6	16 bit	h'18000000 ~ h'19FFFFFF	PC CARD area	Card controller Model: MR-SHPC-01 V2T (Marubun)	
		h'1A000000 ~ h'1A7FFFFF	UART area (ChA)	UART Model: ST16C2550CQ48 (EXAR)	Used as interface with H8/3048F-ONE
		h'1A800000 ~ h'1AFFFFFF	UART area (ChB)	Same as above	Used as interface with host
		h'1B000000 ~ h'1BFFFFFF	ID register area		Reads DIP switch settings
Area 7	-	h'1C000000 ~ h'1FFFFFFF	-	-	Reserved

3.3.3 SH7780 T-Engine memory map

SH7760 T-Engine memory map

Table 3.3.2 shows the SH7760's memory map.

As shown in Table 3.3.2, the expansion board can be expanded to three areas: Area 2, Area 4, and Area 5. Since the wait number and bus width for each area can be set by configuring the bus controller inside the SH7760, devices with different access speeds and different bus widths can be used together.

Table 3.3.2: SH7760 memory map

Area No.	Bus width	Space	Space name	Device	Notes
Area 0	16 bit	h'00000000 ~ h'00FFFFFF	Flash memory area	Real Size:8 MB	
		h'01000000 ~ h'03FFFFFF	Unused area	-	-
Area 1	8/16/32 bit	h'04000000 ~ h' 07FFFFFF	Expansion area	User Expansion Area	Expansion slot CS2# assertion
Area 2/ Area 3	32 bit	h'08000000 ~ h'0FFFFFFF	DDR-SDRAM area	128MB	
Area 4	8/16/32 bit	h'10000000 ~ h'13FFFFFF	Expansion area	User Expansion Area	Expansion slot CS4# assertion
Area 5	8/16/32 bit	h'14000000 ~ h'17FFFFFF	Expansion area	User Expansion Area	Expansion slot CS5# assertion
Area 6	16 bit	h'18000000 ~ h'18FFFFFF	SIM area	Smart Card I/F Area	eTRON
		h'19000000 ~ h'19FFFFFF	PLD register area	PLD register area	USB Interrupt
		h'1A000000 ~ h'1A7FFFFF	UART area (ChA)	UART XR16L2550IM-F(EXAR) x 1	Used as interface with H8/3048F-ONE
		h'1A800000 ~ h'1AFFFFFF	UART area (ChB)		Used as interface with host
		h'1B000000 ~ h'1BFFFFFF	ID register area		Reads DIP switch settings
Area 7	-	h'1C000000 ~ h'1FFFFFFF	-	-	Reserved

3.4. Power supply to the expansion board

3.4.1. Capacity of power supply available from SH77XX T-Engine

Table 3.4.1 shows the voltage and current of the power supply available from an SH77XX T-Engine to the expansion board. If the expansion board needs power in excess of this supply, additional steps must be taken to provide a power supply on the expansion board.

The power supply figures shown in Table 3.4.1 are for reference purposes only and are not guaranteed.

Table 3.4.1: Voltage and current of the power supply available from an SH77XX T-Engine to an expansion board

Expansion bus connector signal	Voltage output	Allowable current	Notes
3.3 V	3.3 V	250 mA	3.3 V: Supplied when SH7727 power is on
3.3 VSB			3.3 VSB: Supplied at all times when a battery or an AC adapter is connected
5 V	5 V	250 mA	Supplied when SH7727 power is on

Notes

- Allowable current refers to the total of 3.3 V and 3.3 VSB currents.
- When a peripheral connected to the T-Engine via USB runs on the bus power, and when a PC card (5 V) is used, the current consumed by the peripheral device and card is subtracted from the maximum allowable current to calculate the real allowable current..

3.5. Interrupt inputs from the expansion board

SH77XX T-Engine features four interrupt input terminals (/IRQ0 - /IRQ3) on the expansion bus connector, for use in input of interrupts from the expansion board. Figure 3.5.1 shows the structure of the expansion bus connector interrupt terminals on a T-Engine. Table 3.5.1 shows the interrupt levels of each interrupt terminal.

Each interrupt terminal in the expansion bus connector recognizes low-level interrupts. After recognition of an interrupt, it is converted to an IRL interrupt within the FPGA on the T-Engine and an interrupt is issued to the SH77XX.

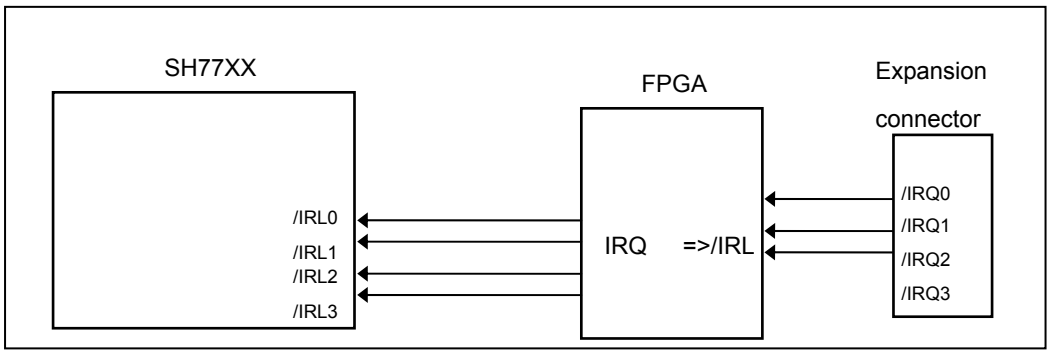


Figure 3.5.1: T-Engine expansion bus connector interrupt terminal structure

Table 3.5.1: Interrupt levels for each interrupt terminal

№	Source of interrupt request	SH77XX Interrupt input terminal	SH7727/SH7720 Interrupt signal level	SH7760 Interrupt signal level	Notes	
					Interrupt level	
					SH7727/ SH7780	SH7760
1	Expansion bus connector /IRQ0 (*1)	/IRL[3..0]	/IRL[3..0]=1101	/IRL[3:0]=0000	2	15
0 0 2	Expansion bus connector /IRQ1 (*1)	/IRL[3..0]	/IRL[3..0]=1001	/IRL[3:0]=0100	6	11
3	Expansion bus connector /IRQ2 (*1)	/IRL[3..0]	/IRL[3..0]=0101	/IRL[3:0]=0111	10	8
4	Expansion bus connector /IRQ3 (*1)	/IRL[3..0]	/IRL[3..0]=0001	/IRL[3:0]=1001	14	6

*1: The interrupt signal level for expansion bus connectors /IRQ0 - 3 is the active low level.

3.6. Expansion board stacking numbers

Use care with regard to power capacity when stacking multiple expansion boards.

Figure 3.6.1 shows an expansion board stacking structure.

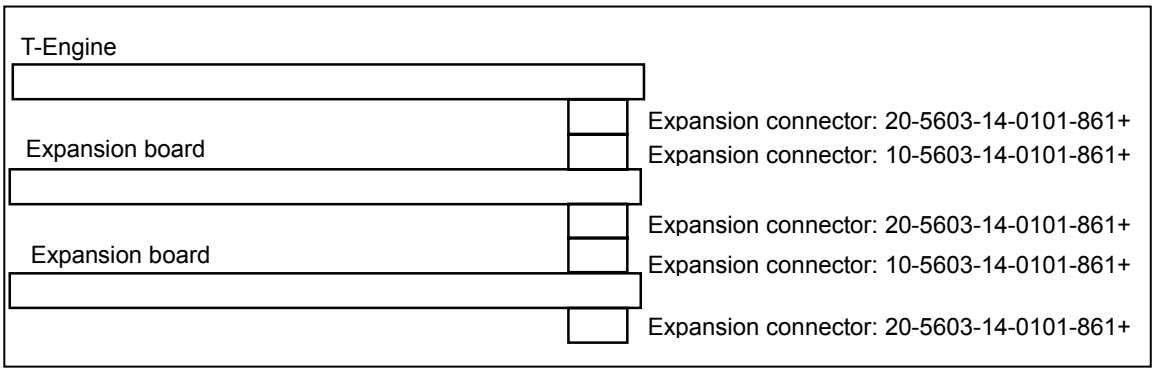


Figure 3.6.1: Expansion board stacking structure

3.7. /WAIT inputs

A SH7727/SH7760 T-Engine has one /WAIT input terminal on its expansion bus connector, for expansion board /WAIT input. When outputting a WAIT signal from the expansion board use open collector output to prevent collision between /WAIT outputs when stacking multiple expansion boards. The /WAIT terminal on the T-Engine side is pulled up at 680Ω. Figure 3.7.1 shows a structural diagram for the /WAIT terminals in an expansion bus connector.

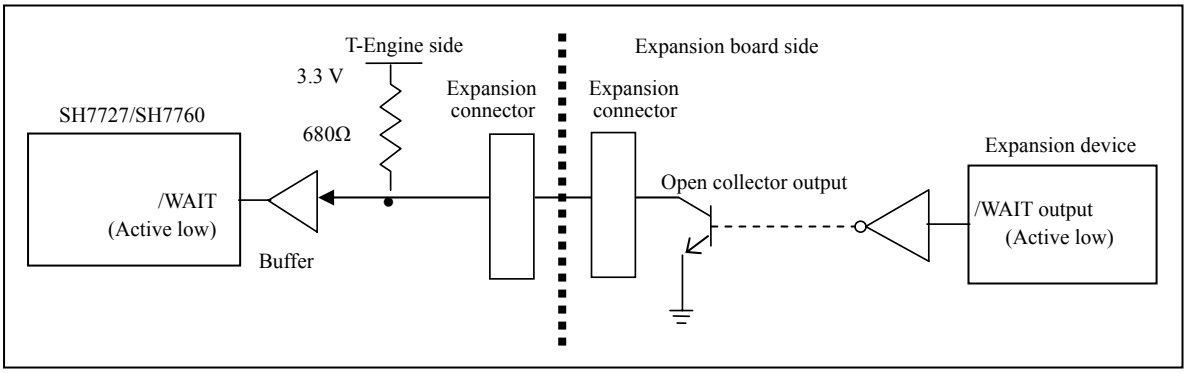


Figure 3.7.1: Structural diagram for /WAIT terminal in expansion bus connector

3.8. AC timing

As shown in Figure 3.8.1, the SH7727/SH7760 bus signals output to the expansion bus connector are output via the bus buffer. For this reason, the bus signal is delayed by approximately 10 nsec vs. the AC timing of the SH7727/SH7760 bus. Be sure to take this delay into account when designing an expansion board. Figure 3.8.2 shows the basic bus timing of an SH7727, while Figure 3.8.3 shows the basic bus timing of an SH7760.

For details of SH7727/SH7760 bus timing, refer to the respective hardware manuals.

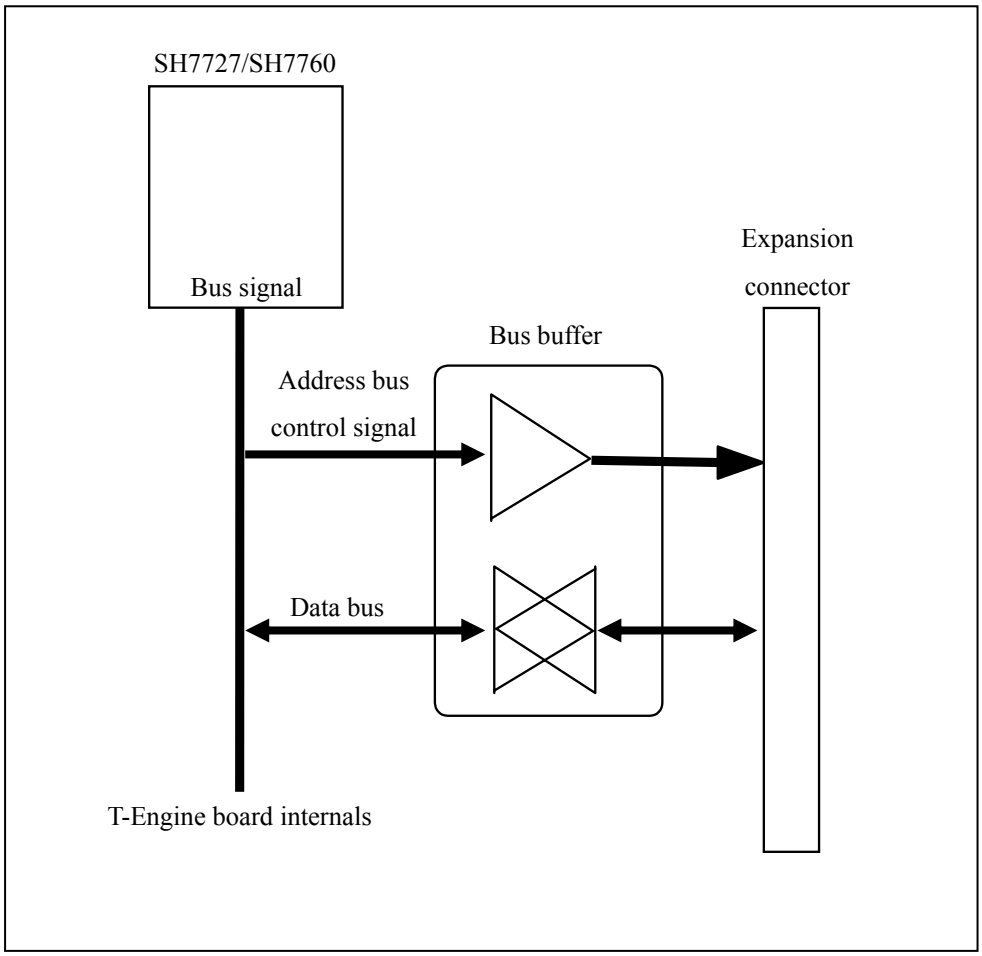


Figure 3.8.1: Expansion bus connector bus buffer structure

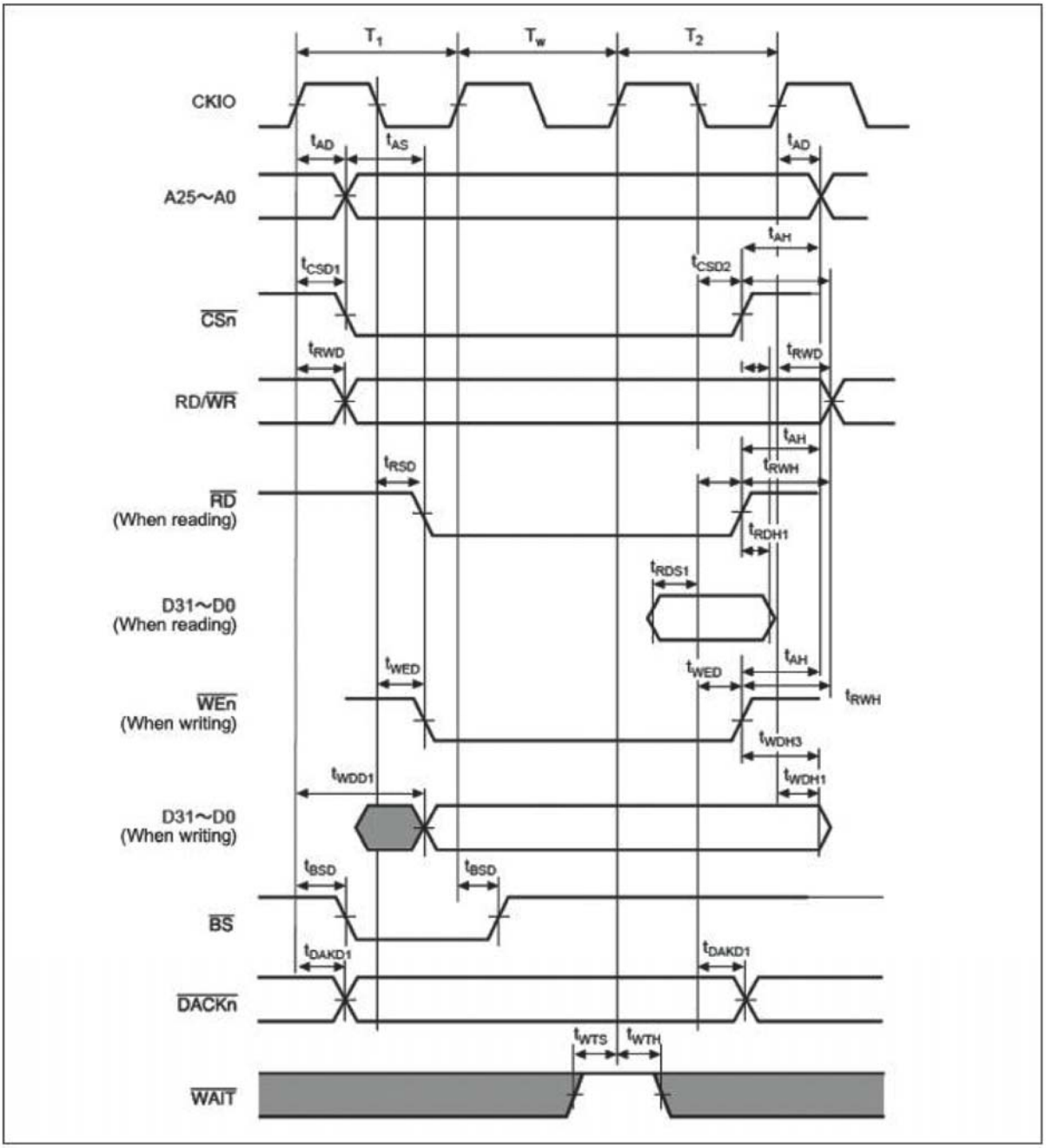


Figure 3.8.2: SH7727 basic bus cycle (one wait state)

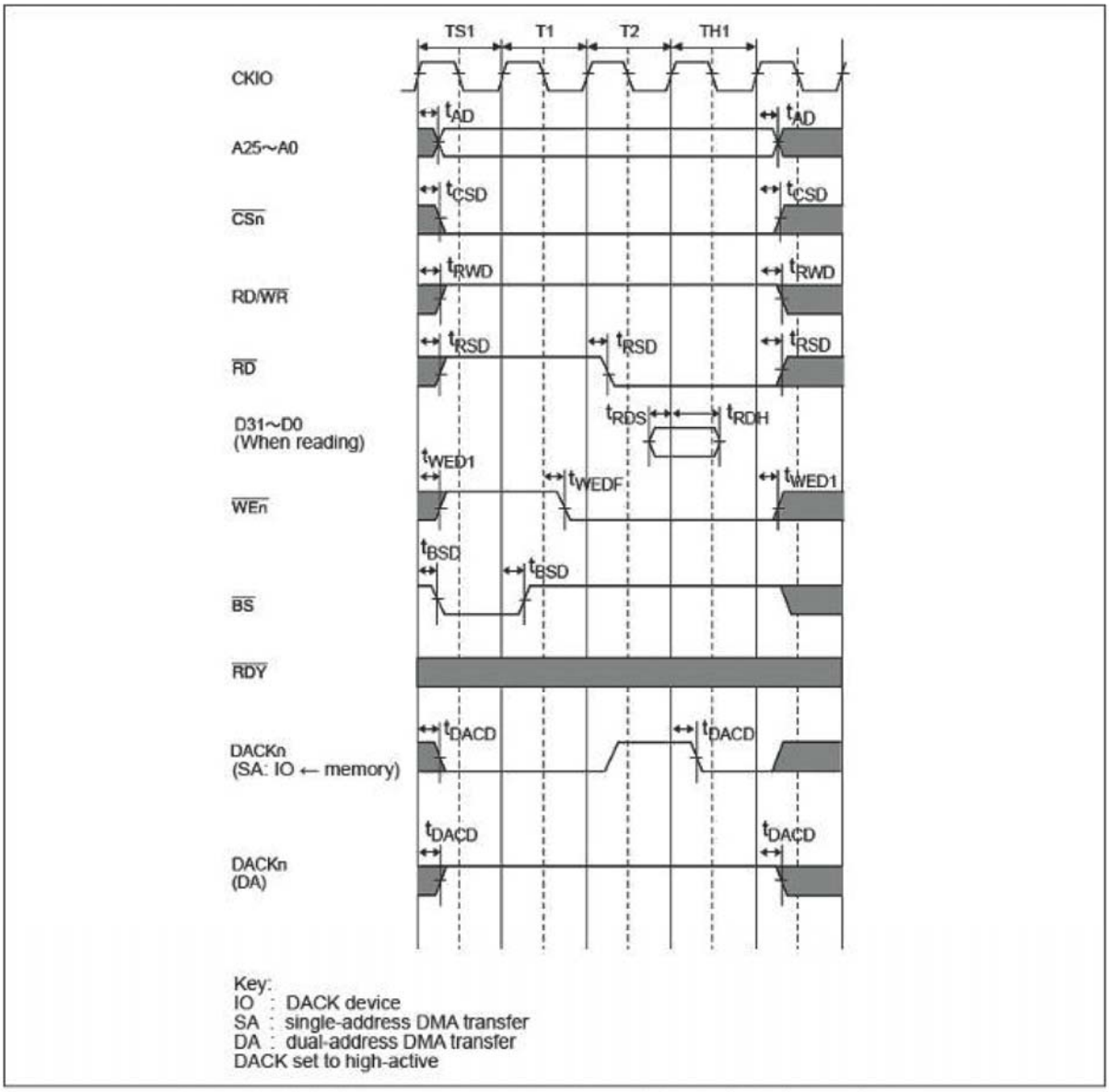


Figure 3.8.3: Memory byte control SRAM bus cycle basic read cycle
(no wait state; address setup/hold time inserted; AnS =1、AnH=1)

■ Chapter 4 SH7751R T-Engine expansion board design guidelines

This chapter describes design guidelines for expansion boards connecting via SH7751R T-Engine expansion slots.

The expansion board refers to a board featuring user selected devices etc. and controllable using the SH7751R address bus, data bus, and PCI bus output to the T-Engine expansion bus connector.

4.1. Expansion bus connector specifications

T-Engine connector type implemented: 20-5603-14-0401-861+ (Kyocera Elco)

Compatible connector type: 10-5603-14-0401-861+ (Kyocera Elco)

Figure 4.1 shows the arrangement of the expansion bus connector.

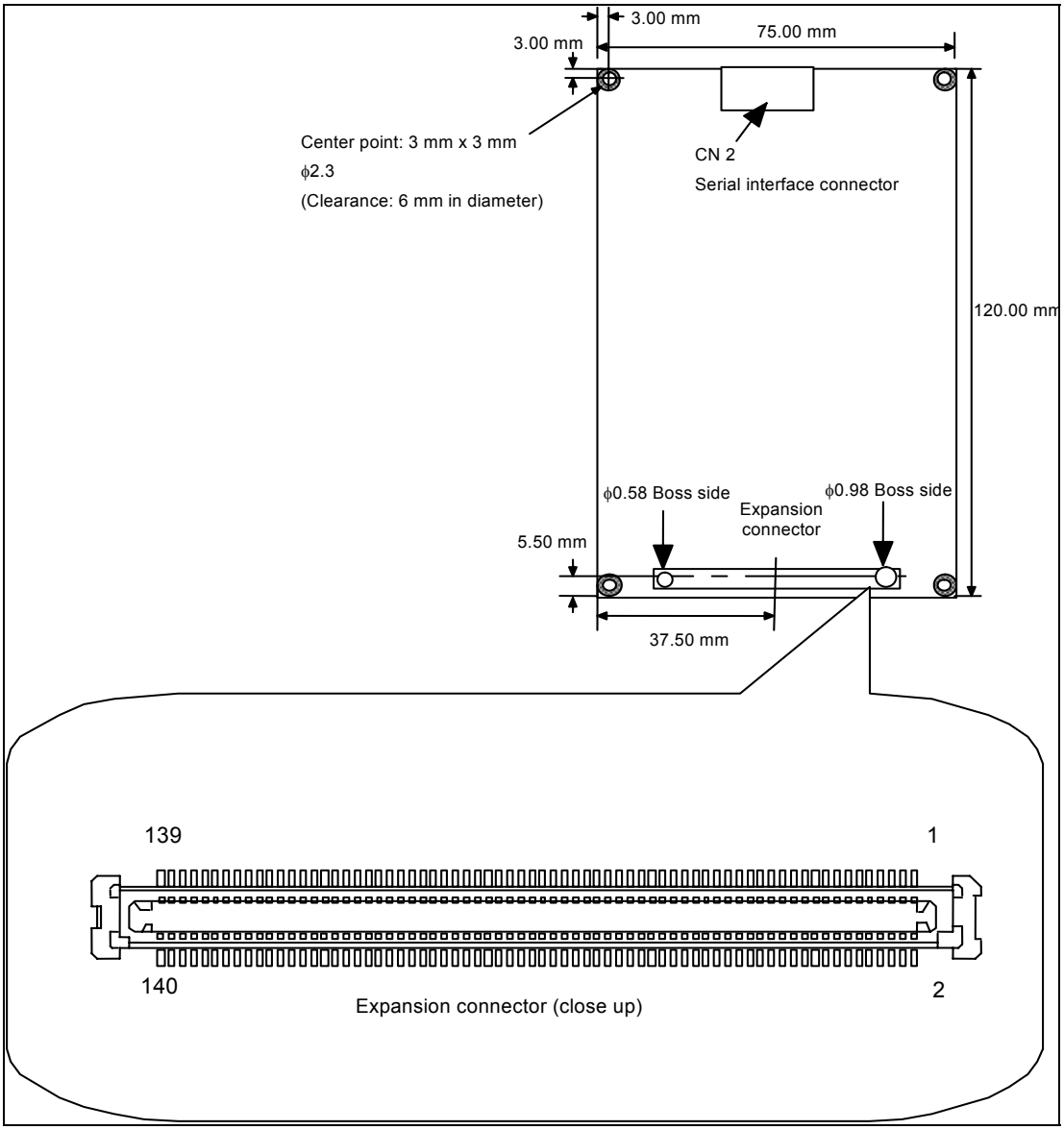


Figure 4.1: Expansion bus connector arrangement

4.2. Expansion bus connector signal arrangement

Table 4.2.1 shows the arrangement of expansion slot signals.

Both PCI bus and local bus signals are used. The electrical power level is 3.3 V.

Table 4.2.1: Expansion slot signal arrangement

Pin No.	信号名	I/O	Pin No.	信号名	I/O	Pin No.	信号名	I/O	Pin No.	信号名	I/O
1	GND	-	36	AD20	I/O	71	AD2	I/O	106	A1	OUT
2	PCLK2	OUT	37	GND	-	72	AD3	I/O	107	A8	OUT
3	GND	-	38	AD18	I/O	73	GND	-	108	A0	OUT
4	PCLK1	OUT	39	GND	-	74	AD1	I/O	109	RESV	-
5	GND	-	40	AD17	I/O	75	GND	-	110	WR#	OUT
6	PCLK0	OUT	41	CBE3#	I/O	76	AD0	I/O	111	GND	-
7	REQ2#	IN	42	AD16	I/O	77	PCIRST#	OUT	112	RD#	OUT
8	VCCIO *2	-	43	CBE2#	I/O	78	LOBAT	-	113	D15	I/O
9	REQ1#	IN	44	STOP#	I/O	79	MPOWER	OUT	114	D7	I/O
10	VCCIO *2	-	45	LOCK#	I/O	80	INTA#	IN	115	D14	I/O
11	REQ0#	IN	46	PERR#	I/O	81	WAKEUP	IN	116	D6	I/O
12	GNT2#	OUT	47	IRDY#	I/O	82	INTB#	IN	117	D13	I/O
13	GND	-	48	TRDY#	I/O	83	INT1#	IN	118	D5	I/O
14	GNT1#	OUT	49	GND	-	84	INTC#	IN	119	D12	I/O
15	GND	-	50	FRAME#	I/O	85	INT2#	IN	120	D4	I/O
16	GNT0#	OUT	51	GND	-	86	INT0#	IN	121	D11	I/O
17	AD31	I/O	52	DEVSEL#	I/O	87	A17	OUT	122	D3	I/O
18	IDSEL2	OUT	53	PAR	I/O	88	CS1#	OUT	123	D10	I/O
19	AD30	I/O	54	SERR#	I/O	89	A16	OUT	124	D2	I/O
20	IDSEL1	OUT	55	CBE1#	I/O	90	CS0#	OUT	125	D9	I/O
21	AD29	I/O	56	AD15	I/O	91	A15	OUT	126	D1	I/O
22	IDSEL0	OUT	57	CBE0#	I/O	92	IORDY	IN	127	D8	I/O
23	AD27	I/O	58	AD14	I/O	93	GND	-	128	D0	I/O
24	AD28	I/O	59	AD12	I/O	94	A7	OUT	129	VBAT *1	-
25	GND	-	60	AD13	I/O	95	A14	OUT	130	VBAT *1	-
26	AD26	I/O	61	GND	-	96	A6	OUT	131	VBAT *1	-
27	GND	-	62	AD11	I/O	97	A13	OUT	132	VBAT *1	-
28	AD25	I/O	63	GND	-	98	A5	OUT	133	VBAT *1	-
29	AD23	I/O	64	AD10	I/O	99	A12	OUT	134	VBAT *1	-
30	AD24	I/O	65	AD8	I/O	100	A4	OUT	135	VBAT *1	-
31	AD22	I/O	66	AD9	I/O	101	A11	OUT	136	VBAT *1	-
32	CS2#	OUT	67	AD6	I/O	102	A3	OUT	137	GND	-
33	AD21	I/O	68	AD7	I/O	103	A10	OUT	138	GND	-
34	EPCE#	OUT	69	AD4	I/O	104	A2	OUT	139	GND	-
35	AD19	I/O	70	AD5	I/O	105	A9	OUT	140	BRD_IN# *3	-

Blue PCI bus Green Local bus
Orange Power Control Reverse Power

*1: When power is supplied from an AC adapter, a 5.6 V (typ.) power supply is provided.

*2: When the SH7751R unit's power is on, power of 3.3 V (typ.) is supplied.

*3: By setting this terminal to the low level, the SH7751R's local bus will be output to the expansion slot. Normally, set this terminal to the low level on the expansion board side.

*4: The PCI bus is output to the expansion slot at all times.

4.3. Areas over which the expansion board can be expanded

Table 4.3.1 shows the SH7751R's memory map.As shown in Table 4.3.1, the expansion board can be expanded to three areas: Area 1, Area 4, and Area 5.Since the wait number and bus width for each area can be set by configuring the bus controller inside the SH7751R, devices with different access speeds and different bus widths can be used together.

Table 4.3.1: SH7751R memory map

Area No.	Bus width	Space	Space name	Device	Note
Area 0	16bit	h'00000000 ~ h'007FFFFF	Flash memory area	8 MB MBM29DL640E90TN (Fujitsu) x 1	
		h'00800000 ~ h'00FFFFFF	-	Flash memory area image	
		h'01000000 ~ h'01FFFFFF	-	Unused area	
		h'02000000 ~ h'03FFFFFF	-	Unused area	
Area 1	16bit	h'04000000 ~ h'0403FFFF	Expansion area (CS0)	256 kB Expansion board expansion area 0 Can be used freely by user via expansion slot (/CS0)	
		h'04040000 ~ h'07FFFFFF		Expansion area (CS0) image	
Area 2	16bit	h'08000000 ~ h'083FFFFF	LCD controller area	LCD controller Model: S1D13806F00A (NEC)	
		h'084000000 ~ h'0BFFFFFF		LCD controller area (image)	
Area 3	32bit	h'0C000000 ~ h'0FFFFFFF	SDRAM area	64 MB EDS2516APTA-75 (ELPIDA) x 2	
Area 4	16bit	h'10000000 ~ h'1003FFFF	Expansion area (CS1)	256 kB Expansionboard expansion area 1 Can be used freely by user via expansion slot (/CS1)	
		h'10040000 ~ h'13FFFFFF		Expansion area (CS1) image	
Area 5	16bit	h'14000000 ~ h'1403FFFF	Expansion area (CS2)	256 kB Expansionboard expansion area 2 Can be used freely by user via expansion slot (/CS2)	
		h'14040000 ~ h'17FFFFFF		Expansion area (CS0) image	
Area 6	16bit	h'18000000 ~ h'19FFFFFF	PC CARD area	Card controller Model: MR-SHPC-01 V2T (Marubun)	
		h'1A000000 ~ h'1A7FFFFF	UART area (ChA)	UART Model: ST16C2550CQ48 (EXAR)	Used as interface with H8/3048F-ONE
		h'1A800000 ~ h'1AFFFFFF	UART area (ChB)	Same as above	Used as serial interface with host
		h'1B000000 ~ h'1B7FFFFF	SIOF area	SIOF Configured in FPGA	

		h'1B800000 ~ h'1BFFFFFF	ID register area		Reads dip-switch settings
Area 7	-	h'1C000000 ~ h'1FFFFFFF	-	-	Reserved

4.4. Power supply to the expansion board

Table 4.4.1 shows the voltage and current of the power supply available from a T-Engine to the expansion board. If the expansion board needs power in excess of this supply, additional steps must be taken to provide a power supply on the expansion board.

The power supply figures shown in Table 4.4.1 are for reference purposes only and are not guaranteed.

Table 4.4.1: Voltage and current of the power supply available to an expansion board

Expansion slot signal	Voltage output	Allowable current	Notes
VCCIO	3.3 V	250 mA	Supplied when SH7751R power is on
VBAT	5.6 V	3.0 A	Supplied at all times when an AC adapter is connected

4.5. Interrupt inputs from the expansion board

Figure 4.5.1 shows the structure of the interrupt signals on an SH7751R unit.

Table 4.5.1 shows the level correspondence for each interrupt signal.

As shown in Figure 4.5.1, interrupt signals from each device on a T-Engine board is converted to an /IRL signal in the FPGA and then the SH7751R's /IRL [3.:0] is output.

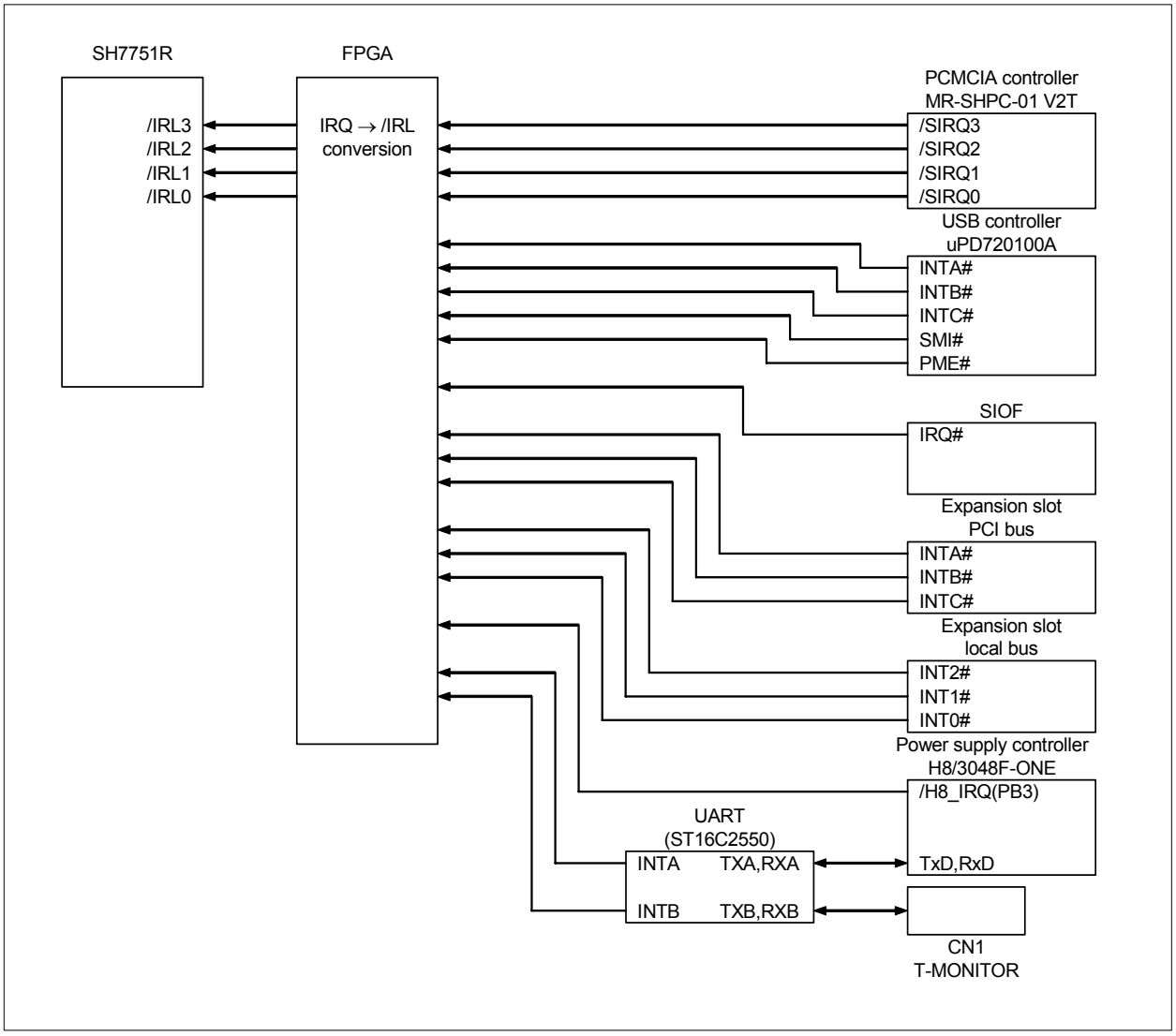


Figure 4.5.1: T-Engine expansion bus connector interrupt terminal structure

Table 4.5.1: Level correspondence for each interrupt signal

No	Source of interrupt request	Interrupt input terminal	Interrupt signal level	Notes
1	PC CARD controller (SIRQ3)	/IRL[3:0]	/IRL[3:0] = 0010	Interrupt level 13
2	PC CARD controller (SIRQ2)	/IRL[3:0]	/IRL[3:0] = 0101	Interrupt level 10
3	PC CARD controller (SIRQ1)	/IRL[3:0]	/IRL[3:0] = 1000	Interrupt level 7
4	PC CARD controller (SIRQ0)	/IRL[3:0]	/IRL[3:0] = 1110	Interrupt level 1
5	USB controller (INTA#)	/IRL[3:0]	/IRL[3:0] = 1001	Interrupt level 6
6	USB controller (INTC#)	/IRL[3:0]	/IRL[3:0] = 1001	Interrupt level 6
7	SIOF	/IRL[3:0]	/IRL[3:0] = 1010	Interrupt level 4
8	UART controller ChA	/IRL[3:0]	/IRL[3:0] = 1011	Interrupt level 4
9	UART controller ChB	/IRL[3:0]	/IRL[3:0] = 0100	Interrupt level 11
10	H8/3048F-ONE	/IRL[3:0]	/IRL[3:0] = 0011	Interrupt level 12
11	PCI bus (INTA#)	/IRL[3:0]	/IRL[3:0] = 0000	Interrupt level 15
12	PCI bus (INTB#)	/IRL[3:0]	/IRL[3:0] = 0110	Interrupt level 9
13	PCI bus (INTC#)	/IRL[3:0]	/IRL[3:0] = 1100	Interrupt level 3
14	Expansion slot (INT2#)	/IRL[3:0]	/IRL[3:0] = 1101	Interrupt level 2
15	Expansion slot (INT1#)	/IRL[3:0]	/IRL[3:0] = 0111	Interrupt level 8
16	Expansion slot (INT0#)	/IRL[3:0]	/IRL[3:0] = 0001	Interrupt level 14
17	LCD controller (Ysync)	/IRL[3:0]	/IRL[3:0] = 0101	Interrupt level 10

4.6. Expansion board stacking numbers

Use care with regard to power capacity when stacking multiple expansion boards.

Figure 4.6.1 shows an expansion board stacking structure.

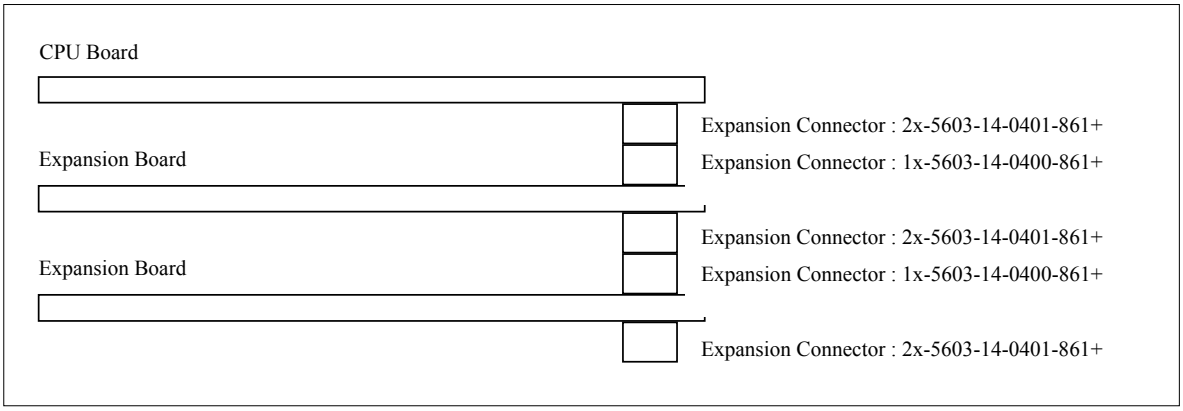


Figure 4.6.1: Expansion board stacking structure

4.7. Expansion board IORDY outputs

The expansion slot on the T-Engine board features one IORDY input terminal for Expansion board IORDY input use. When outputting an IORDY signal from a Expansion board, be sure to use open collector output to prevent collisions between IORDY outputs when stacking multiple Expansion boards.

The IORDY terminal on the T-Engine side is pulled up at 680Ω. Figure 4.7.1 shows a structural diagram for the IORDY terminal in an expansion slot.

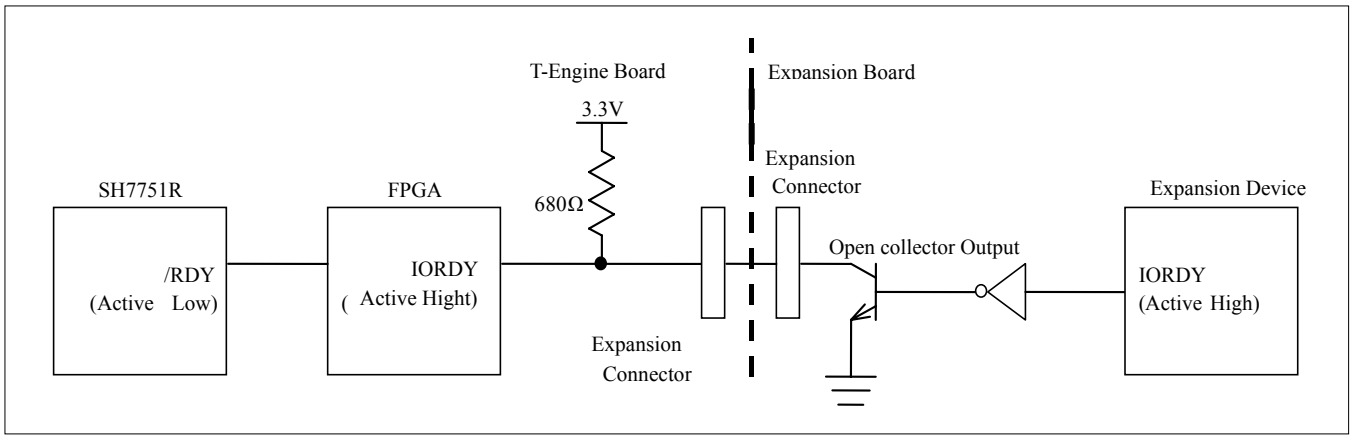


Figure 4.7.1: Structural diagram for IORDY terminal in an expansion slot

4.8. AC timing

As shown in Figure 4.8.1, the SH7751R bus signals output to the expansion slot are output via the bus buffer. For this reason, the bus signal is delayed by approximately 10 nsec vs. the AC timing of the SH7751R bus. Be sure to take this delay into account when designing a Expansion board. Figure 4.8.2 shows the basic bus timing of an SH7751R. For details of SH7751R bus timing, refer to the SH7751R hardware manual.

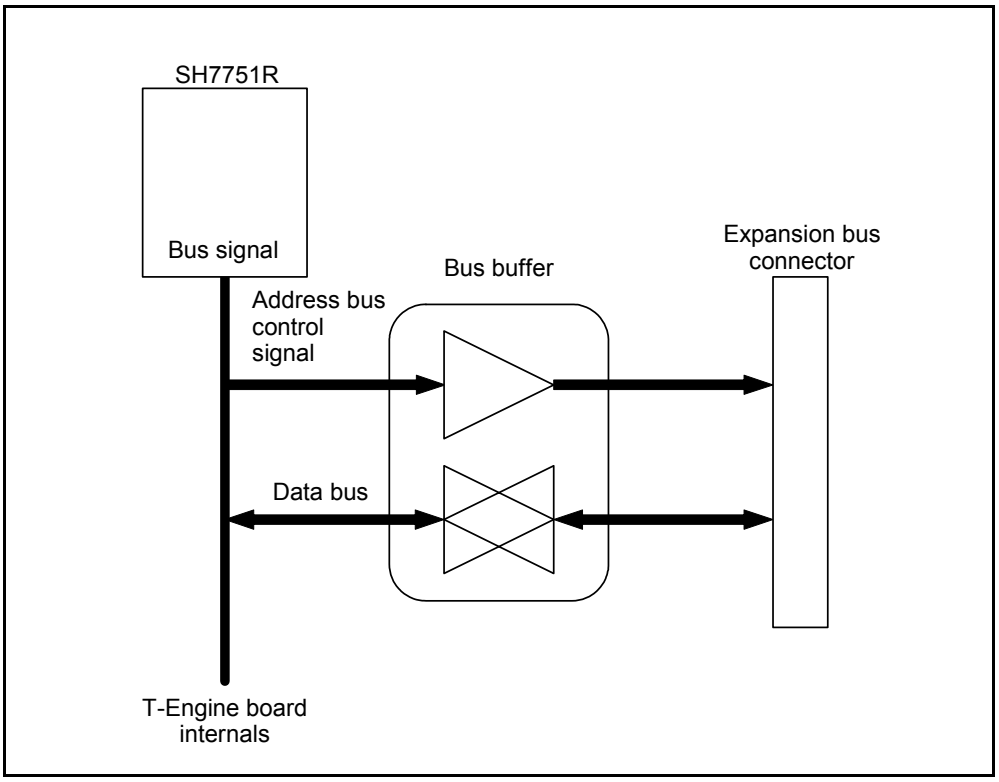


Figure 4.8.1: Expansion bus connector bus buffer structure

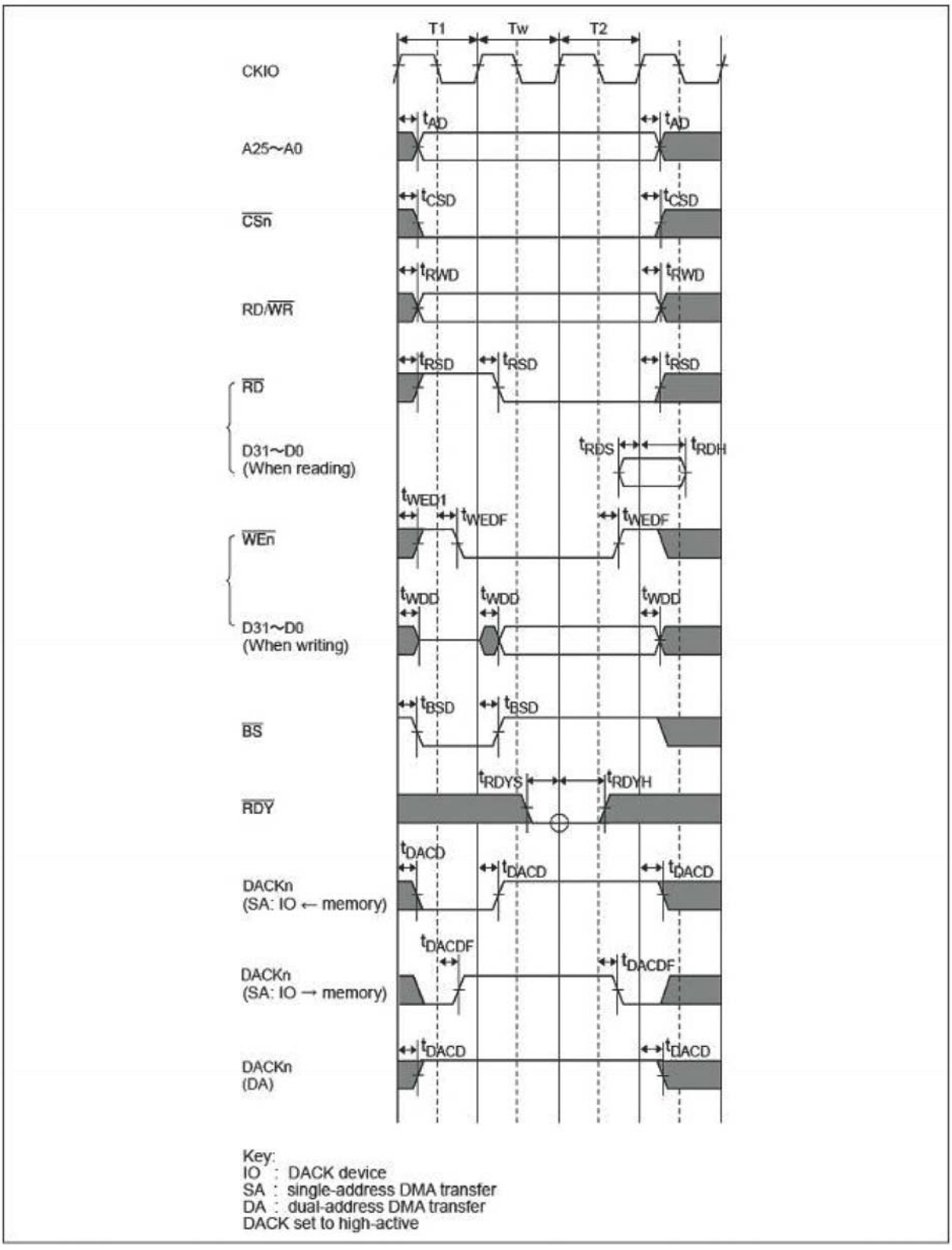


Figure 4.8.2: SH7751R basic cycle (one wait state)

■ Chapter 5 SH7145 expansion board design guidelines

This chapter describes design guidelines for expansion boards connecting via SH7145 μT-Engine expansion slots.

The expansion board refers to a board featuring user selected devices etc. and controllable using the SH7145 address bus, data bus, and control signals or serial (start-stop synchronization) signals output to the μT-Engine expansion bus connector.

5.1. SH7145 μT-Engine expansion bus connector specifications

μT-Engine connector type implemented: 20-5603-14-0102-861+ (Kyocera Elco)

Compatible connector type: 10-5603-14-0102-861+ (Kyocera Elco)

Figure 5.2.1 shows the arrangement of the expansion bus connector.

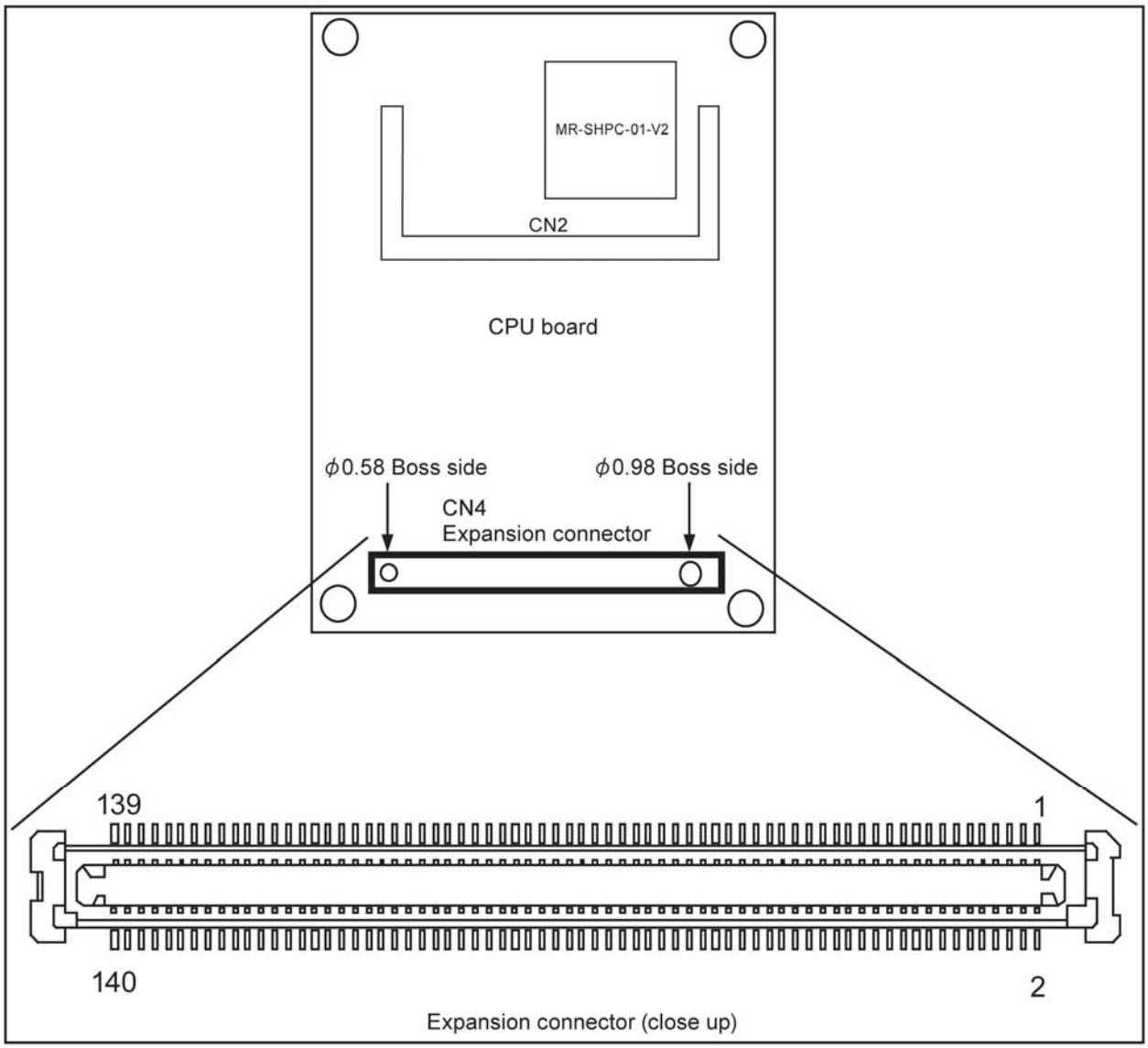


Figure 5.2.1: Expansion bus connector arrangement

5.2. Expansion bus connector signal arrangement

Table 5.2.1 shows the arrangement of expansion slot signals.

Table 5.2.1: Expansion slot signal arrangement

Pin No.	Signal	I/O	Pin No.	Signal	I/O	Pin No.	Signal	I/O	Pin No.	Signal	I/O
1	-	-	36	PD29	O	71	-	-	106	-	-
2	-	-	37	PD30	O	72	-	-	107	-	-
3	-	-	38	PD31	O	73	_EPROMCE	O	108	DBGMD	I
4	-	-	39	GND	-	74	_CS3	O	109	GND	-
5	D0	I/O	40	GND	-	75	-	-	110	GND	-
6	D1	I/O	41	CK	O	76	PE13/TIOC4B	O	111	TCK	I
7	D2	I/O	42	GND	-	77	PE14/TIOC4C	O	112	TMS	I
8	D3	I/O	43	GND	-	78	PE15/TIOC4D	O	113	_TRST	I
9	D4	I/O	44	GND	-	79	GND	-	114	TDI	I
10	D5	I/O	45	A0	O	80	GND	-	115	TDO	O
11	D6	I/O	46	A1	O	81	_RD	O	116	_ASEBRKAK	O
12	D7	I/O	47	A2	O	82	_WAIT	I	117	3.3VSB	-
13	D8	I/O	48	A3	O	83	_WRL	O	118	3.3VSB	-
14	D9	I/O	49	A4	O	84	_WRH	O	119	3.3VSB	-
15	D10	I/O	50	A5	O	85	-	-	120	3.3VSB	-
16	D11	I/O	51	A6	O	86	-	-	121	PE0/TIOC0A	O
17	D12	I/O	52	A7	O	87	GND	-	122	PE1/TIOC0B	O
18	D13	I/O	53	A8	O	88	GND	-	123	PE2/TIOC0C	O
19	D14	I/O	54	A9	O	89	-	-	124	PE3/TIOC0D	O
20	D15	I/O	55	A10	O	90	-	-	125	PE6/TIOC2A	O
21	GND	-	56	A11	O	91	-	-	126	-	-
22	GND	-	57	A12	O	92	_IRQ3	I	127	3.3V	-
23	PD16	O	58	A13	O	93	NMI_IN	I	128	3.3V	-
24	PD17	O	59	A14	O	94	_RES_IN	I	129	3.3V	-
25	PD18	O	60	A15	O	95	_RES_OUT	O	130	3.3V	-
26	PD19	O	61	GND	-	96	-	-	131	3.3V	-
27	-	-	62	GND	-	97	-	-	132	3.3V	-
28	PD21	I/O	63	A16	O	98	-	-	133	VBAT_IN	-
29	CONT1	O	64	A17	O	99	_ROMSEL	I	134	VBAT_IN	-
30	CONT2	O	65	A18	O	100	-	-	135	VBAT_IN	-
31	_DREQ0	I	66	A19	O	101	GND	-	136	VBAT_IN	-
32	PD25	I/O	67	A20	O	102	GND	-	137	GND	-
33	DACK0	O	68	A21	O	103	SCI_TXD3	O	138	GND	-
34	PD27	I/O	69	-	-	104	SCI_RXD3	I	139	GND	-
35	PD28	O	70	-	-	105	-	-	140	GND	-

5.3. Areas over which the expansion board can be expanded

Table 5.3.1 shows the SH7145's memory map in the SH7145 μT-Engine.

As shown in Table 5.3.1, the expansion board can be expanded to the CS3 space.

The wait number for the CS3 space can be set by configuring the bus controller inside the SH7145.

Table 5.3.1: SH7145 memory map

Area	Bus width	Space	Device	Notes
CS0 space	16bit	h'00000000 ~ h'000FFFFF	Flash memory 1 MB MBM29LV800TA70PBT (Fujitsu) x 1	Software wait = 3 External wait = 0 Idle cycle = 1
		h'00100000 ~ h'002FFFFF	—	
		h'00300000 ~ h'003FFFFF	SRAM 1 MB TC55VEM316AXBN55 (Toshiba) x 1	
CS1 space	16bit	h'00400000 ~ h'004000FF	SD card interface controller MN5774 (Matsushita)	Software wait = 3 External wait = Variable Idle cycle = 1
		h'00400100 ~ h'007FFFFF	Image	
CS2 space	16bit	h'00800000 ~ h'00BFFFFF	CF card interface controller MR-SHPC-01 V2T (Marubun)	Software wait = 5 External wait = Variable Idle cycle = 1
CS3 space	16bit	h'00C00000 ~ h'00FFFFFF	Expansion bus interface	Software wait = Arbitrary External wait = Arbitrary Idle cycle = Arbitrary
Reserve	—	h'01000000 ~ h'FFFF7FFF	—	
Peripheral I/O	—	h'FFFF8000 ~ h'FFFFBFFF	—	
Reserve	—	h'FFFFC000 ~ h'FFFFDFFF	—	
On-board RAM	—	h'FFFFE000 ~ h'FFFFFFFF	On-board RAM 8 kB	

5.4. Power supply to expansion board

Table 5.4.1 shows the voltage and current of the power supply available from a μT-Engine to the expansion board. If the expansion board needs power in excess of this supply, additional steps must be taken to provide a power supply on the expansion board.

The power supply figures shown in Table 5.4.1 are for reference purposes only and are not guaranteed.

Table 5.4.1: Voltage and current of the power supply available to an expansion board

Expansion slot signal	Voltage output	Allowable current	Notes
3.3 V	3.3 V	250 mA	3.3 V: Supplied when SH7145 power is on
3.3 VSB			3.3 VSB: Supplied at all times when an AC adapter is connected

- Allowable current refers to the total of 3.3 V and 3.3 VSB currents.
- When the μT-Engine uses a Compact Flash card, the current consumed by the device and the card is subtracted from the maximum allowable current, to caluculate the real allowable current. For example, when using 3.3 V/100 mA as the power supply to the Compact Flash card, the 3.3 V allowable current that can be used by the expansion slot is 150 mA (250 mA - 100 mA).

5.5. Interrupt inputs from the expansion board

μT-Engine features an _IRQ3 interrupt input terminal on the expansion bus connector, for use in input of interrupts from the expansion board.

Table 5.5.1 shows the interrupt levels for each interrupt terminal.

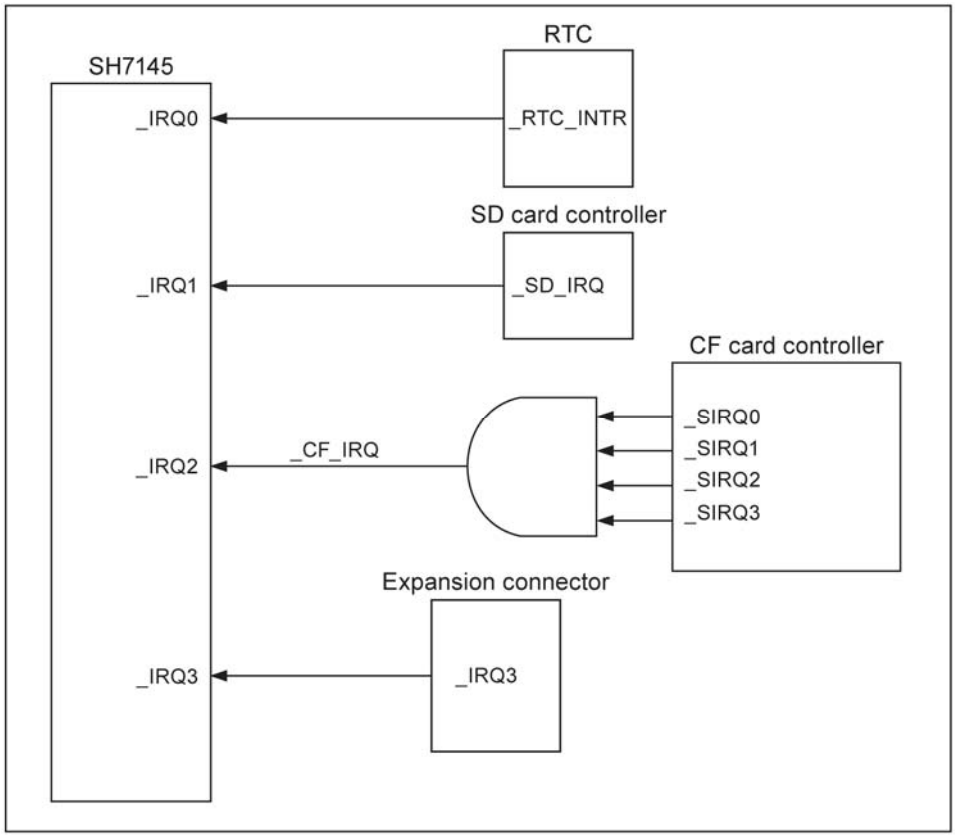


Figure 5.5.1: μT-Engine interrupt terminal structure

Table 5.5.1: Interrupt levels for each interrupt terminal

No.	Source of interrupt request	Interrupt input terminal	Interrupt signal level	Notes
1	RTC controller	_IRQ0	Active low	
2	SD card controller	_IRQ1	Active low	
3	PC CARD controller	_IRQ2	Active low	
4	Expansion slot/IRQ3	_IRQ3	Active low	

5.6. Expansion board stacking numbers

Use care with regard to power capacity when stacking multiple expansion boards.

Figure 5.6.1 shows an expansion board stacking structure.

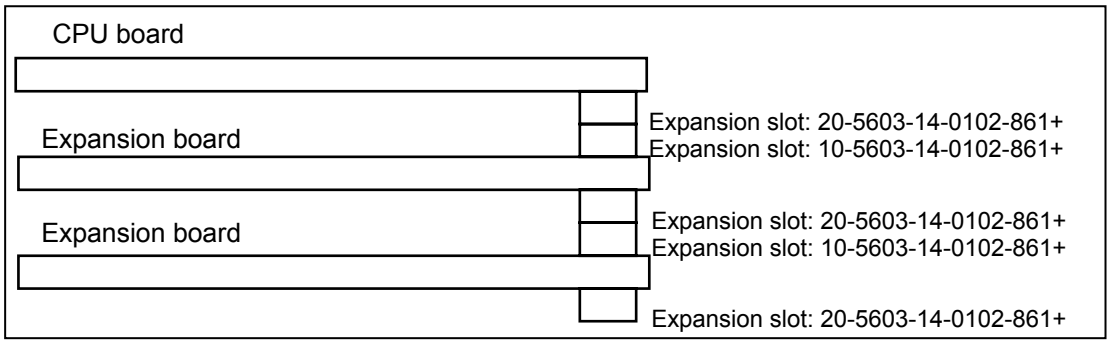


Figure 5.6.1: Expansion board stacking structure

5.7. /WAIT inputs

µT-Engine has one /WAIT input terminal on its expansion bus connector, for expansion board /WAIT input.

When outputting a WAIT signal from the expansion board, be sure to use open collector output to prevent collision between /WAIT outputs when stacking multiple expansion boards. The /WAIT terminal on the µT-Engine side is pulled up at 680Ω. Figure 5.7.1 shows a structural diagram for the /WAIT terminals in an expansion bus connector.

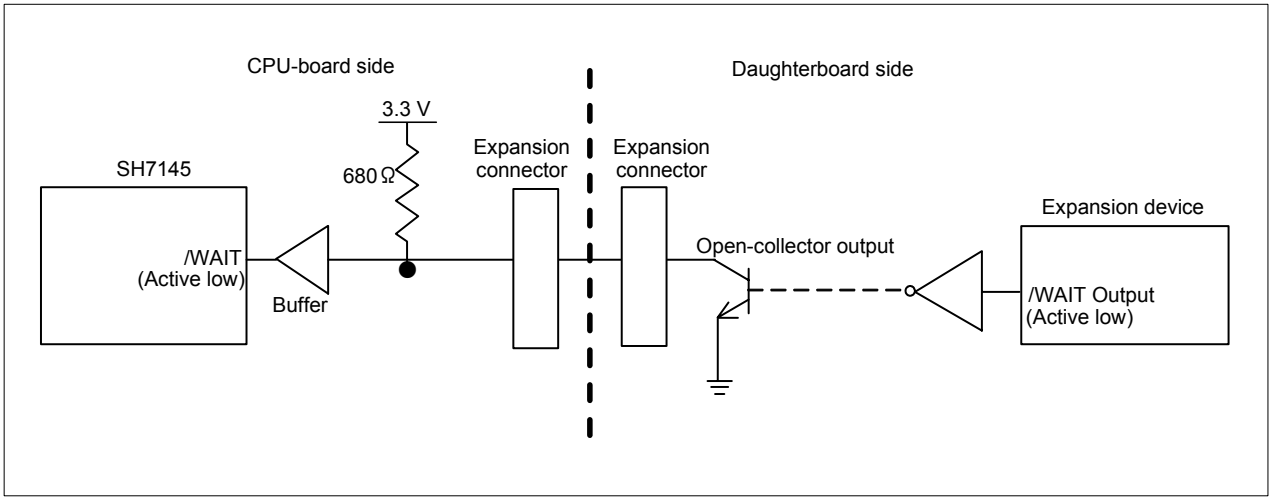


Figure 5.7.1: Structural diagram for /WAIT terminal in expansion slot

■ Chapter 6 M32104/M32192μT-Engine expansion board design guidelines

This chapter describes design guidelines for expansion boards connecting via the expansion bus connectors on M32104/M32192 μT-Engine boards.

The expansion board refers in general to a Expansion board used for functional expansion by connecting via the expansion bus connector on a μT-Engine board. By connecting the M32104/M32192 address bus, data bus, bus control signals, and I/O ports on the expansion bus connector to a customer's hardware IP, the μT-Engine board can be used as a component for hardware-IP testing and execution.

6.1. M32104/M32192 μT-Engine expansion bus connector specifications

6.1.1. Types of expansion bus connectors

Expansion boards can be stacked with a μT-Engine board using the following expansion bus connectors. Expansion bus connectors come in two types: PLUG and RECE. Only the RECE connector is implemented on the μT-Engine board.

Be sure to install a PLUG connector on the μT-Engine board side and a RECE connector on the opposite side for stacking expansion boards. The manufacturer and model numbers for the expansion bus connectors are shown below:

1 PLUG: Kyocera Elco 14 5603 14 0202 861+
2 RECE: Kyocera Elco 24 5603 14 0202 861+

Although both T-Engine and μT-Engine use connectors with the same external shape, their signal arrangements differ. For this reason, incorrect insertion is prevented using the key structure (protrusions inside the connectors).

The key structure can be identified using the key code ("xxxx" in "24 5603 14 xxxx 861"). This product uses the key code 0202. The following two types of connectors can be connected to this connector: those with the key code 0202 and those with the key code 0000 (the master key code, denoting a product that can connect to all connectors).

6.1.2. Stacking expansion boards

Up to two expansion boards may be stacked. Use care with regard to the power capacity (up to 3.3 V, 400 mA) for stacked expansion boards.

Figure 6.1.2 shows an example of stacking expansion boards.

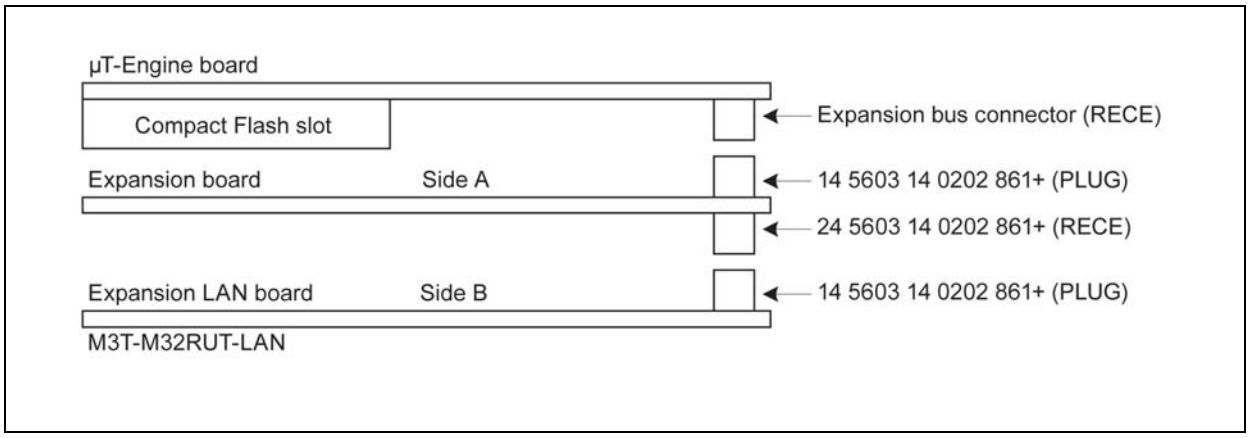


Figure 6.1.2: Example of stacking expansion boards

6.1.3. Expansion board size

It is recommended that an expansion board have the same size (85 mm x 60 mm) as a μT-Engine board.

Be sure not to install any components greater than 2 mm in height on side A (the CPU board side) of the expansion board.

Be sure not to install any components greater than 7 mm in height on side B (the expansion LAN board side) of the expansion board. However, for a bottom board on which only a PLUG will be installed, with no expansion LAN board used, components less than 15 mm in height may be installed on side B.

Rules concerning board dimensions are summarized below.

Use a board thickness of 1.6 mm.

Place a hole 2.1 mm in diameter in each of the four corners of the board, for use in installing the board. Center each hole 2.5 mm from the edge of the board. Be sure not to install any components or patterns (other than GND) within the area 2.5 mm in radius from the center of each hole.

Center the expansion bus connector's boss hole 5.5 mm from the edge of the board. Center the expansion bus connector on the center of the board.

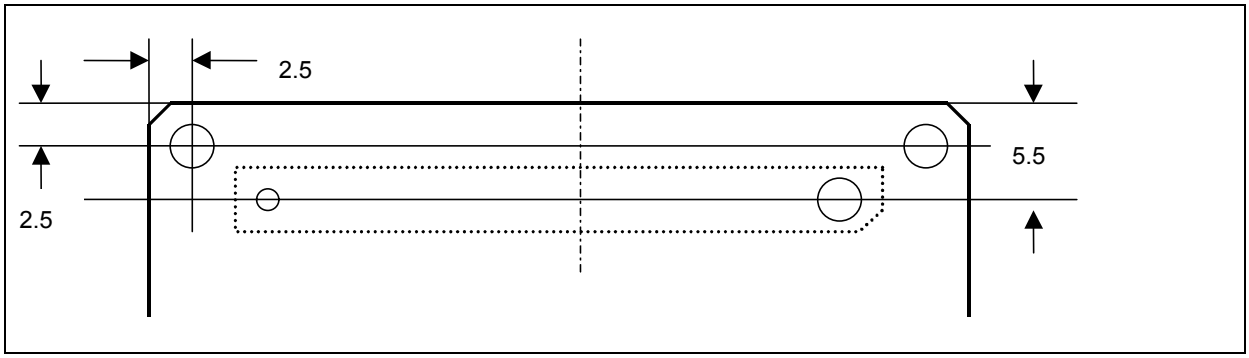


Figure 6.1.3: Dimensions around the expansion bus connector

6.1.4. Direction in which to install the expansion bus connector

Figure 6.1.4 shows the direction in which to install the expansion bus connector. Use care when designing patterns, because the pin numbers of the connector are the reverse of the pin numbers of the component as designated by the connector manufacturer.

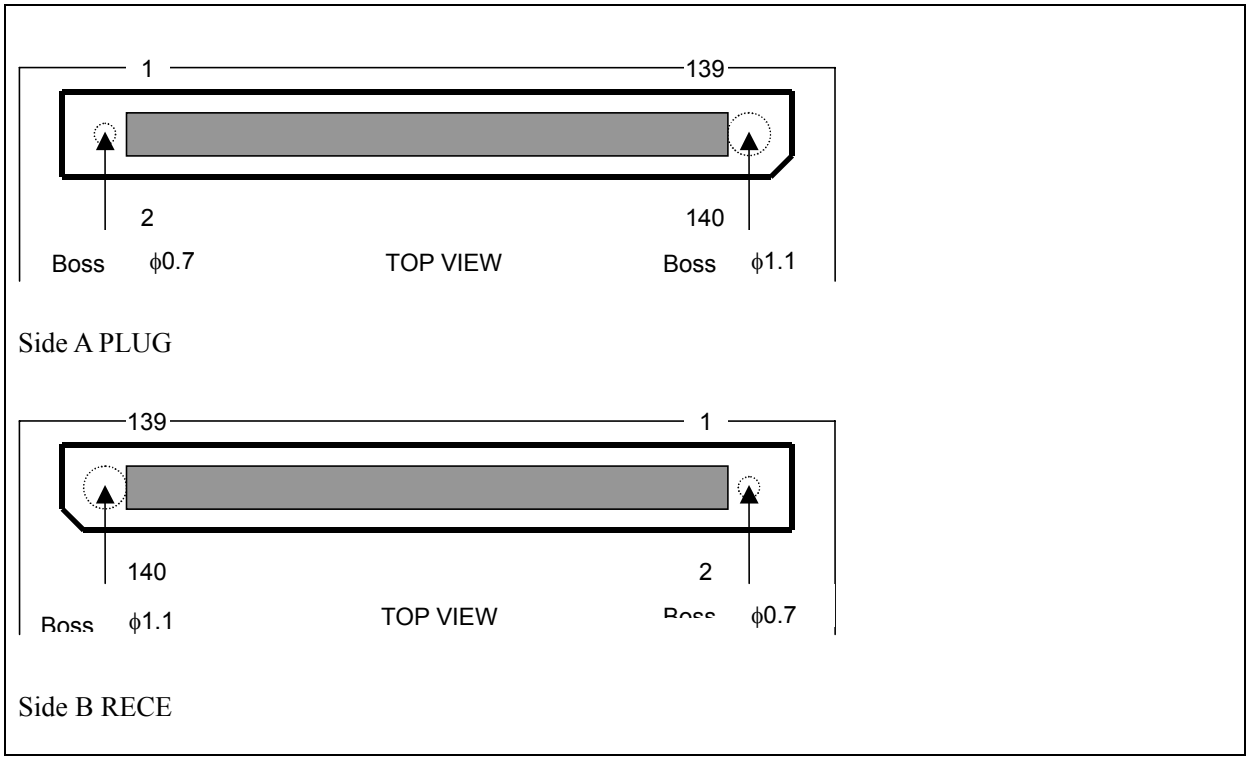


Figure 6.1.4: Direction in which to install the expansion bus connector

6.2. Expansion bus signal arrangement

6.2.1. Expansion bus signal arrangement

Table 6.2.1 shows the arrangement of expansion bus signals.

Table 6.2.1: Expansion bus signal arrangement (1/4)

No.	Expansion bus signal	M32104 μT-Engine signal	M32192 μT-Engine signal	I/O	Pull up or down	Buffer
1	GND	GND	GND	-	-	-
2	GND	GND	GND	-	-	-
3	GND	GND	GND	-	-	-
4	GND	GND	GND	-	-	-
5	V33 (3.3 V power supply)	V33 (3.3 V power supply)	V33 (3.3 V power supply)	-	-	-
6	V33 (3.3 V power supply)	V33 (3.3 V power supply)	V33 (3.3 V power supply)	-	-	-
7	V33 (3.3 V power supply)	V33 (3.3 V power supply)	V33 (3.3 V power supply)	-	-	-
8	V33 (3.3 V power supply)	V33 (3.3 V power supply)	V33 (3.3 V power supply)	-	-	-
9	JTAG_RST#	JTAG_RST#	JTAG_RST#	IN	-	N
10	TRST#	TRST#	TRST#	IN	UP	N
11	TMS	TMS	TMS	IN	UP	N
12	TDO	TDO	TDO	OUT	-	N
13	TDI	TDI	TDI	IN	UP	N
14	TCK	TCK	TCK	IN	DOWN	N
15	GND	GND	GND	-	-	-
16	GND	GND	GND	-	-	-
17	P77	P77	P83	I/O	UP	N
18	P76	P76	P85	I/O	UP	N
19	Reserve	NC	NC	-	UP	N
20	Reserve	NC	NC	-	UP	N
21	P67	P67	P93	I/O	UP	N
22	P66	P66	P82	I/O	UP	N
23	P65	P65	P84	I/O	UP	N
24	P64	P64	P86	I/O	UP	N
25	P63	P63	P94	I/O	UP	N
26	P62	P62	P87	I/O	UP	N
27	GND	GND	GND	-	-	-
28	GND	GND	GND	-	-	-
29	P27	P27	P95	I/O	UP	N
30	P26	P26	NC	I/O	UP	N
31	P25	P25	NC	I/O	UP	N
32	P24	P24	P96	I/O	UP	N
33	EXTPWR (External power supply)	NC	NC	-	-	-
34	EXTPWR (External power supply)	NC	NC	-	-	-
35	V33SB (Reserve power supply)	NC	NC	-	-	-

Table 6.2.1: Expansion bus signal arrangement (2/4)

No.	Expansion bus signal	M32104 μT-Engine signal	M32192 μT-Engine signal	I/O	Pull up or down	Buffer
36	V33SB (Reserve power supply)	NC	NC	-	-	-
37	GND	GND	GND	-	-	-
38	GND	GND	GND	-	-	-
39	INT3#	NC	TIN27	IN	-	N
40	INT2#	NC	TIN18	IN	-	N
41	BBSEL6#	NC	NC	OUT	-	N
42	BBSEL5#	NC	NC	OUT	-	N
43	SW2	SW2	SW2	OUT	UP	N
44	SW1	SW1	SW1	OUT	UP	N
45	LED2	LED2	LED2	OUT	DOWN	N
46	LED1	LED1	LED1	OUT	DOWN	N
47	GND	GND	GND	-	-	-
48	GND	GND	GND	-	-	-
49	EXREADY#	EXREADY#	MPU_WAIT# *1	IN	DOWN	N
50	EXINT	EXINT	TIN24	IN	UP	N
51	BCS1#	BCS1#	BUS_CS# *1	OUT	UP	Y
52	BWS3#	BWS3#	NC	OUT	-	Y
53	BWS2#	BWS2#	NC	OUT	-	Y
54	BWS1#	BWS1#	BUS_BLW# *1	OUT	-	Y
55	BWS0#	BWS0#	BUS_BHW# *1	OUT	-	Y
56	BRS#	BRS#	BUS_RD# *1	OUT	-	Y
57	GND	GND	GND	-	-	-
58	GND	GND	GND	-	-	-
59	GND	GND	GND	-	-	-
60	EXCLK	EXCLK	BCLK	OUT	-	Y
61	GND	GND	GND	-	-	-
62	GND	GND	GND	-	-	-
63	RESET#	RESET#	RESET#	OUT	-	N
64	GND	GND	GND	-	-	-
65	GND	GND	GND	-	-	-
66	BA30	BA30	BA30	OUT	-	Y
67	BA29	BA29	BA29	OUT	-	Y
68	BA28	BA28	BA28	OUT	-	Y
69	BA27	BA27	BA27	OUT	-	Y
70	BA26	BA26	BA26	OUT	-	Y

*1: This signal is generated in the control PLD rather than directly by the MCU.

Table 6.2.1: Expansion bus signal arrangement (3/4)

No.	Expansion bus signal	M32104 μT-Engine signal	M32192 μT-Engine signal	I/O	Pull up or down	Buffer
71	BA25	BA25	BA25	OUT	-	Y
72	BA24	BA24	BA24	OUT	-	Y
73	GND	GND	GND	-	-	-
74	GND	GND	GND	-	-	-
75	BA23	BA23	BA23	OUT	-	Y
76	BA22	BA22	BA22	OUT	-	Y
77	BA21	BA21	BA21	OUT	-	Y
78	BA20	BA20	BA20	OUT	-	Y
79	BA19	BA19	BA19	OUT	-	Y
80	BA18	BA18	BA18	OUT	-	Y
81	BA17	BA17	BA17	OUT	-	Y
82	BA16	BA16	BA16	OUT	-	Y
83	GND	GND	GND	-	-	-
84	GND	GND	GND	-	-	-
85	BA15	BA15	BA15	OUT	-	Y
86	BA14	BA14	BA14	OUT	-	Y
87	BA13	BA13	BA13	OUT	-	Y
88	BA12	BA12	BA12	OUT	-	Y
89	BA11	BA11	BA11	OUT	-	Y
90	BA10	BA10	BA10	OUT	-	Y
91	BA9	BA9	BA9	OUT	-	Y
92	BA8	BA8	BA8 (Fixed to “L”)	OUT	-	Y
93	GND	GND	GND	-	-	-
94	GND	GND	GND	-	-	-
95	BD31	BD31	NC	I/O	-	Y
96	BD30	BD30	NC	I/O	-	Y
97	BD29	BD29	NC	I/O	-	Y
98	BD28	BD28	NC	I/O	-	Y
99	BD27	BD27	NC	I/O	-	Y
100	BD26	BD26	NC	I/O	-	Y
101	BD25	BD25	NC	I/O	-	Y
102	BD24	BD24	NC	I/O	-	Y
103	GND	GND	GND	-	-	-
104	GND	GND	GND	-	-	-
105	BD23	BD23	NC	I/O	-	Y

Table 6.2.1: Expansion bus signal arrangement (4/4)

No.	Expansion bus signal	M32104 μT-Engine signal	M32192 μT-Engine signal	I/O	Pull up or down	Buffer
106	BD22	BD22	NC	I/O	-	Y
107	BD21	BD21	NC	I/O	-	Y
108	BD20	BD20	NC	I/O	-	Y
109	BD19	BD19	NC	I/O	-	Y
110	BD18	BD18	NC	I/O	-	Y
111	BD17	BD17	NC	I/O	-	Y
112	BD16	BD16	NC	I/O	-	Y
113	GND	GND	GND	-	-	-
114	GND	GND	GND	-	-	-
115	BD15	BD15	BD15	I/O	-	Y
116	BD14	BD14	BD14	I/O	-	Y
117	BD13	BD13	BD13	I/O	-	Y
118	BD12	BD12	BD12	I/O	-	Y
119	BD11	BD11	BD11	I/O	-	Y
120	BD10	BD10	BD10	I/O	-	Y
121	BD9	BD9	BD9	I/O	-	Y
122	BD8	BD8	BD8	I/O	-	Y
123	GND	GND	GND	-	-	-
124	GND	GND	GND	-	-	-
125	BD7	BD7	BD7	I/O	-	Y
126	BD6	BD6	BD6	I/O	-	Y
127	BD5	BD5	BD5	I/O	-	Y
128	BD4	BD4	BD4	I/O	-	Y
129	BD3	BD3	BD3	I/O	-	Y
130	BD2	BD2	BD2	I/O	-	Y
131	BD1	BD1	BD1	I/O	-	Y
132	BD0	BD0	BD0	I/O	-	Y
133	V33 (3.3 V power supply)	V33 (3.3 V power supply)	V33 (3.3 V power supply)	-	-	-
134	V33 (3.3 V power supply)	V33 (3.3 V power supply)	V33 (3.3 V power supply)	-	-	-
135	V33 (3.3 V power supply)	V33 (3.3 V power supply)	V33 (3.3 V power supply)	-	-	-
136	V33 (3.3 V power supply)	V33 (3.3 V power supply)	V33 (3.3 V power supply)	-	-	-
137	GND	GND	GND	-	-	-
138	GND	GND	GND	-	-	-
139	GND	GND	GND	-	-	-
140	GND	GND	GND	-	-	-

6.2.2. Expansion bus I/O port allocation

Table 6.2.2 shows a list of I/O port allocations for the μT-Engine board's expansion bus.

Table 6.2.2: List of I/O port allocations for μT-Engine board expansion bus

No.	M32104 μT-Engine signal	M32192 μT-Engine signal	M3T-M32RUT-LAN (REV.B)	M3T-M32RUT-LCD
17	P77/MFT0B/CTS2#/INT12	P83/RXD0/TO25	CTS2 (Port)	NC
18	P76/MFTX0B/RTS2#/INT11	P85/TXD1/TO23	ARXCLK# (Timer output)	NC
19	NC	NC	NC	NC
20	NC	NC	NC	NC
21	P67/RXD2	P93/TO16/SCLKI5/SCLKO5	ARSTART (Port)	NC
22	P66/TXD2	P82/TXD0/TO26	TXD2	NC
23	P65/RD/WR#/SCLK2/INT10	P84/SCLKI0/SCLKO0/TO24	SCLK2	NC
24	P64/RXD1	P86/RXD1/TO22	RXD1	NC
25	P63/TXD1	P94/TO17/TXD5/DD15	XRST# (Port)	NC
26	P62/SCLK1/MFT0A/INT9	P87/SCLKI1/SCLKO1/TO21	SCLK1	NC
29	P27/DMACK0/CTS1#/INT7	P95/TO18/RXD5/DD14	CTS1 (Port)	NC
30	P26/DMREQ0/RTS1#/INT6	NC	NC	INT6_104
31	P25/HLDA#/DMACK1/MFT1B	NC	NC	NC
32	P24/HOLD#/DMREQ1/MFT1A	P96/TO19/DD13	READ (Port)	NC
33	NC	NC	NC	EXTPWR
34	NC	NC	NC	EXTPWR
35	NC	NC	NC	V33SB
36	NC	NC	NC	V33SB
39	NC	P72/HREQ#/TIN27	NC	NC
40	NC	P132/TIN18/DIN2	NC	INT2_700#
41	NC	NC (Fixed to "H")	NC	BBSEL6# (Unused)
42	NC	NC (Fixed to "H")	NC	BBSEL5# (Unused)
49	P55/READY#/MFT2A/INT4	P153/TIN3/WAIT#	EXREADY#	EXREADY#
50	P51/INT0/MFT3A	P103/TO11/TIN24	EXINT	NC

3 The expansion bus connector's EXREADY# can be shared, because it is output from each board using open collector output.

4 On the M32104 μT-Engine board, since BBSEL5# and BBSEL6# use NC signals, the M3T-M32RUT-LCD adds 1 MΩ pull up resistance.

5 The EXREADY# to the M32192 μT-Engine board is delivered after conversion by the control PLD to a WAIT#.

6.3. Areas over which expansion can be conducted

6.3.1. M32104 μT-Engine board

Figure 6.3.1 shows the M32104 memory map for the M32104 μT-Engine board. The expansion board can be allocated to the CS1 area. The wait number and bus width for the CS1 area can be set by configuring the chip select controller inside the M32104.

Address	CS	
H'0000_0000 : H'003F_FFFF	CS0 area (4 MB)	External flash ROM area (4 MB)
H'0040_0000 : H'005F_FFFF	-	Unused area
H'0060_0000 : H'0060_FFFF	-	M32104 on board RAM area (64 KB)
H'0061_0000 : H'006F_FFFF		Use of this area not permitted
H'0070_0000 : H'007F_FFFF	-	M32104 on board SFR area (1 MB)
H'0080_0000 : H'00FF_FFFF	-	Unused area
H'0100_0000 : H'010F_FFFF	CS1 area (16 MB)	Area reserved for expansion LAN board (1 MB)
H'0110_0000 : H'011F_FFFF		Area reserved for expansion Bluetooth board (1 MB)
H'0120_0000 : H'012F_FFFF		Area reserved for expansion FPGA board (1 MB)
H'0130_0000 : H'013F_FFFF		Area reserved for expansion LCD board (1 MB)
H'0140_0000 : H'017F_FFFF		Area reserved for LCD controller (4 MB)
H'0180_0000 : H'01FF_FFFF		Unused area
H'0200_0000 : H'02FF_FFFF	CS3 area (16 MB)	Control PLD area (16 MB)
H'0300_0000 : H'03FF_FFFF	CS2 area (16 MB)	Compact Flash area (16 MB)
H'0400_0000 : H'04FF_FFFF	-	External SDRAM area (16 MB)
H'0500_0000 : H'1FFF_FFFF	-	Unused area

Table 6.3.1: M32104 memory map

6.3.2. M32192 µT-Engine board

Figure 6.3.2 shows the M32192 memory map for the M32192 µT-Engine board.

The expansion board can be allocated to the CS1 area. The wait number and bus width for the CS1 area can be set by configuring the chip-select controller inside the M32192.

Address	CS	
H'0000_0000 : H'000F_FFFF	-	M32192 on board ROM area (1 MB)
H'0010_0000 : H'001F_FFFF	CS0 area (7 MB)	External SRAM area (1 MB)
H'0020_0000 : H'0027_FFFF		Control PLD area (512 KB)
H'0028_0000 : H'002F_FFFF		Compact Flash area (512 KB)
H'0030_0000 : H'007F_FFFF		Use of this area not permitted
H'0080_0000 : H'0080_3FFF	-	SFR area (16 KB)
H'0080_4000 : H'0082_FFFF		M32192 on board RAM area (176 KB)
H'0083_0000 : H'00FF_FFFF		Use of this area not permitted
H'0100_0000 : H'010F_FFFF	CS1 area (8 MB)	Area reserved for expansion LAN board (1 MB)
H'0110_0000 : H'011F_FFFF		Area reserved for expansion Bluetooth board (1 MB)
H'0120_0000 : H'012F_FFFF		Area reserved for expansion FPGA board (1 MB)
H'0130_0000 : H'013F_FFFF		Area reserved for expansion LCD board (1 MB)
H'0140_0000 : H'017F_FFFF		Area reserved for LCD controller (4 MB)
H'0180_0000 : H'01FF_FFFF	-	Use of this area not permitted
H'0200_0000 : H'027F_FFFF	CS2 area (8 MB)	Unused area (8 MB)
H'0280_0000 : H'02FF_FFFF	-	Use of this area not permitted
H'0300_0000 : H'037F_FFFF	CS3 area (8 MB)	Unused area (8 MB)
H'0380_0000 : H'03FF_FFFF	-	Use of this area not permitted

Table 6.3.2: M32192 memory map

6.4. Power supply to the expansion board

6.4.1. Available power supply

Table 6.4.3 shows the power supply available to the expansion board. If the expansion board needs power in excess of this supply, additional steps must be taken to provide a power supply on the expansion board.

The power supply figures shown in Table 6.4.3 are for reference purposes only and are not guaranteed.

Table 6.4.3: Voltage and current of the power supply available to an expansion board

Signal	Voltage output	Allowable current	Notes
V33	3.3 V	400 mA	Supplied when the power is on
V33SB	3.3 V	50 mA	Supplied when an M3T-M32RUT-LCD and an AC adapter/battery are connected
EXTPWR	5.0 V	500 mA	Supplied when an M3T-M32RUT-LCD and an AC adapter are connected

6.4.2. M32104 μT-Engine system power supply

When using the standard structure (i.e., when not attaching the M3T-M32RUT-LCD expansion multimedia board), attach the AC adapter to the M3T-M32RUT-POW power supply board. A V33 power supply will be provided to the M3T-M32104UT-CPU μT-Engine board with an M32104 through a special-purpose connector. Also, a V33 power supply will be provided to the M3T-M32RUT-LAN expansion LAN board through the expansion bus. Note that power is not supplied to the V33SB or the EXTPWR.

When connecting the M3T-M32RUT-LCD, attach the AC adapter to the M3T-M32RUT-LCD. A V33 power supply will be provided to the M3T-M32104UT-CPU and the M3T-M32RUT-LAN through the expansion bus. Note that in this case power is supplied to the V33SB and the EXTPWR.

6.4.3. M32192 μT-Engine system power supply

When using the standard structure (i.e., when not attaching the M3T-M32RUT-LCD expansion multimedia board), attach the AC adapter to the M3T-M32192UT-CAN CAN board. A V33 power supply will be provided to the M3T-M32192UT-CPU μT-Engine board with an M32192 through a special-purpose connector. Also, a V33 power supply will be provided to the M3T-M32RUT-LAN expansion LAN board through the expansion bus. Note that power is not supplied to the V33SB or the EXTPWR.

When connecting the M3T-M32RUT-LCD, attach the AC adapter to the M3T-M32RUT-LCD. A V33 power supply will be provided to the M3T-M32192UT-CPU and the M3T-M32RUT-LAN through the expansion bus. Note that in this case power is supplied to the V33SB and the EXTPWR.

6.5. Interrupt inputs from the expansion board

6.5.1. M32104 μT-Engine

When connecting the M3T-M32RUT-LAN expansion LAN board, use the M32104's INT0 (EXINT).

When connecting the M3T-M32RUT-LCD expansion multimedia board, use the M32104's INT6 (INT6_104).

When connecting both the expansion LAN board and the expansion multimedia board, the microcomputer's INT terminal cannot be secured. One possible alternative is not using the expansion LAN board's AR camera (making INT7, INT9, INT10, INT11, and INT12 available for use) and using a timer interrupt (MFT1B).

6.5.2. M32192 μT-Engine

When connecting the M3T-M32RUT-LAN expansion LAN board, use the M32192's TIN24 (EXINT).

When connecting the M3T-M32RUT-LCD expansion multimedia board, use the M32192's TIN18 (INT2_700#).

TIN27 can be used when connecting both the expansion LAN board and the expansion multimedia board.

6.6. EXREADY# input

An EXREADY# terminal is available for READY# inputs from the expansion board.

When outputting an EXREADY# signal, be sure to use open collector output to prevent collision when stacking multiple expansion boards. In other words, ordinarily output the EXREADY# signal using HiZ, and output “H” only when making the CPU wait.

The EXREADY# signal is pulled down at 1kΩ within the CPU board, and by the control PLD, after 1BCLK either a READY# signal is delivered to the M32104 or a WAIT# signal is delivered to the M32192.

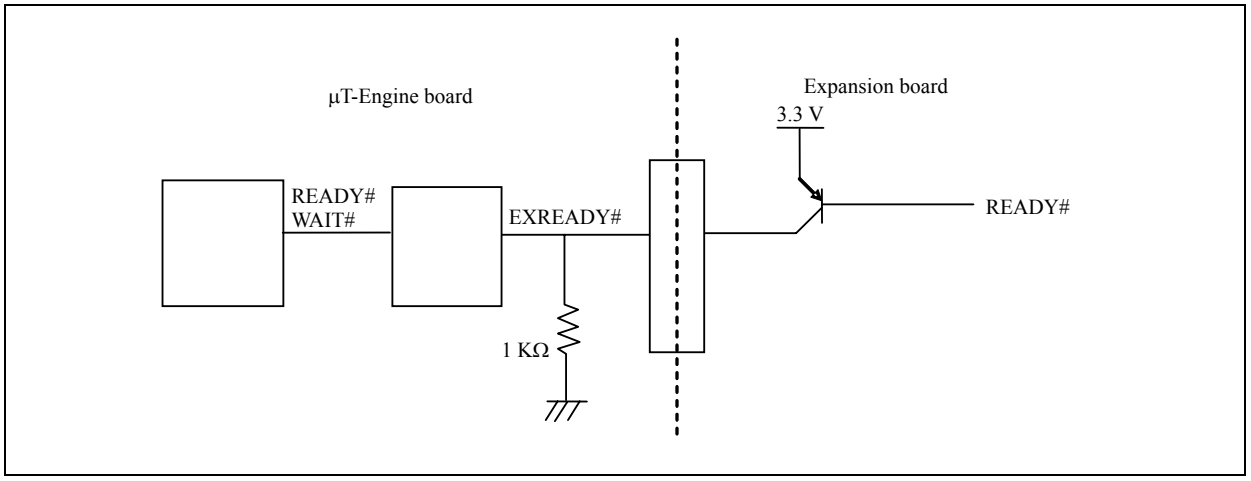


Figure 6.6: EXREADY# input circuitry

■ Chapter 7 VR5500 T-Engine expansion board design guidelines

This chapter describes design guidelines for expansion boards connecting via the expansion slot on a Vr5500 T-Engine.

The expansion board refers to a board featuring user selected devices etc. and controllable using the Vr5500 address bus, data bus, and PCI bus output to the T-Engine expansion bus connector.

7.1. T-Engine expansion bus connector specifications

T-Engine connector type implemented: 20-5603-14-0404-861+ (Kyocera Elco)

Compatible connector type: 10-5603-14-0404-861+ (Kyocera Elco)

Figure 7.1 shows the arrangement of the expansion bus connector.

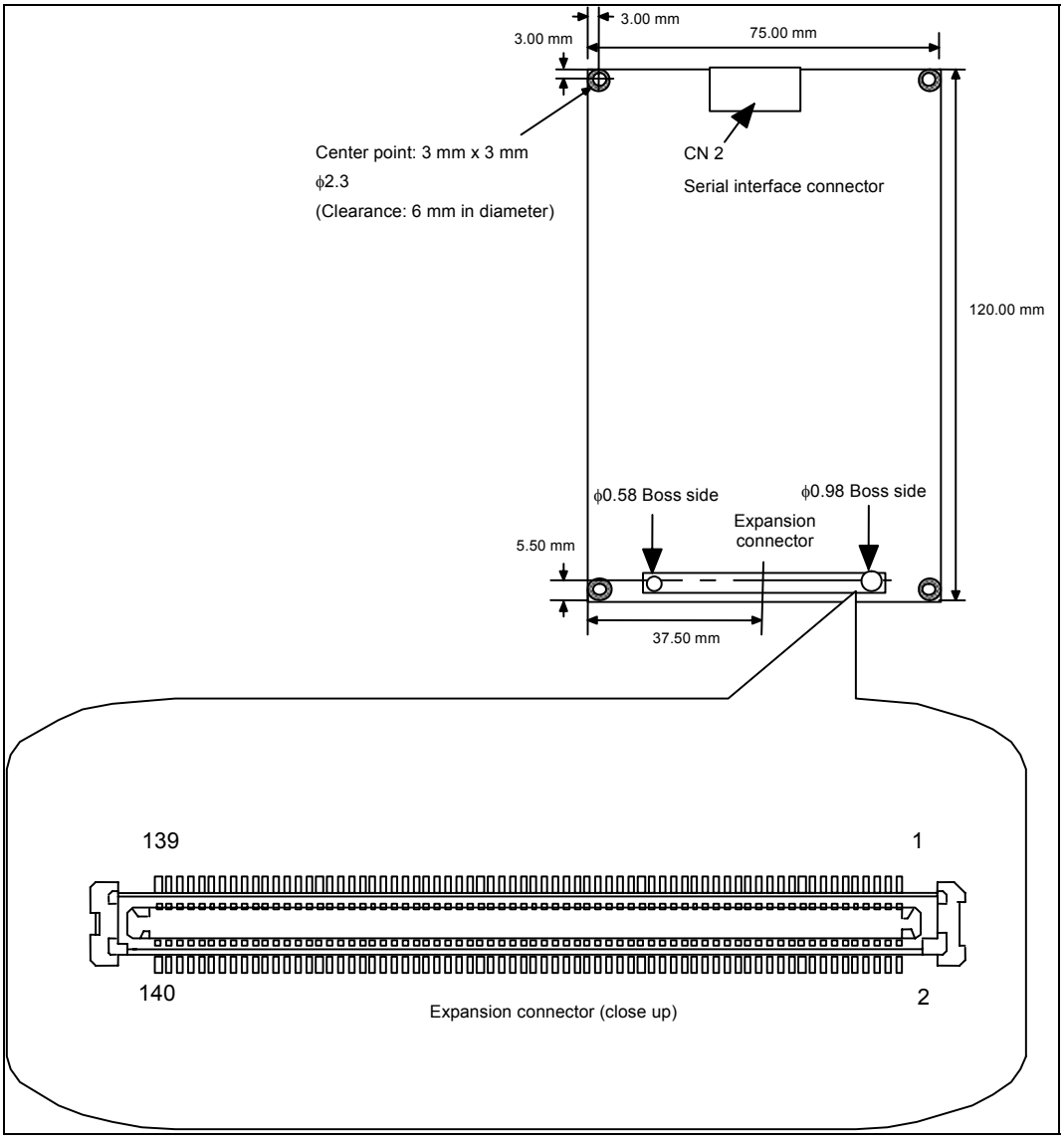


Figure 7.1: Expansion bus connector arrangement

7.2. Expansion bus connector signal arrangement

Table 7.2 shows the arrangement of expansion slot signals.

Both PCI bus and local bus signals are used. The electrical power level is 3.3 V.

Table 7.2: Expansion slot signal arrangement

Pin No.	Signal	I/O	Pin No.	Signal	I/O	Pin No.	Signal	I/O	Pin No.	Signal	I/O
1	GND	-	36	PAD20	I/O	71	PAD2	I/O	106	LA1	OUT
2	PCICLK2	OUT	37	GND	-	72	PAD3	I/O	107	LA8	OUT
3	GND	-	38	PAD18	I/O	73	GND	-	108	LA0	OUT
4	PCICLK1	OUT	39	GND	-	74	PAD1	I/O	109	LWE1#	OUT
5	GND	-	40	PAD17	I/O	75	GND	-	110	LWE0#	OUT
6	PCICLK0	OUT	41	PCI_CBE3#	I/O	76	PAD0	I/O	111	GND	-
7	PCI_REQ2#	IN	42	PAD16	I/O	77	PCI_RESET#	OUT	112	LRD#	OUT
8	3.3V *1	OUT	43	PCI_CBE2#	I/O	78	LOBAT#	IN(O/D)	113	LD15	I/O
9	PCI_REQ1#	IN	44	PCI_STOP#	I/O	79	SHDN#	OUT	114	LD7	I/O
10	3.3V *1	OUT	45	PCI_LOCK#	I/O	80	PCI_INTA#	IN(O/D)	115	LD14	I/O
11	PCI_REQ0#	IN	46	PCI_PERR#	I/O	81	WAKEUP#	IN(O/D)	116	LD6	I/O
12	PCI_GNT2#	OUT	47	PCI_IRDY#	I/O	82	PCI_INTB#	IN(O/D)	117	LD13	I/O
13	GND	-	48	PCI_TRDY#	I/O	83	Reserved	-	118	LD5	I/O
14	PCI_GNT1#	OUT	49	GND	-	84	PCI_INTC#	IN(O/D)	119	LD12	I/O
15	GND	-	50	PCI_FRAME#	I/O	85	Reserved	-	120	LD4	I/O
16	PCI_GNT0#	OUT	51	GND	-	86	Reserved	-	121	LD11	I/O
17	PAD31	I/O	52	PCI_DEVSEL#	I/O	87	LA17	OUT	122	LD3	I/O
18	IDSEL2(PAD29)	OUT	53	PCI_PAR	I/O	88	FCS1#	OUT	123	LD10	I/O
19	PAD30	I/O	54	PCI_SERR#	IN(O/D)	89	LA16	OUT	124	LD2	I/O
20	IDSEL1(PAD28)	OUT	55	PCI_CBE1#	I/O	90	FCS0#	OUT	125	LD9	I/O
21	PAD29	I/O	56	PAD15	I/O	91	LA15	OUT	126	LD1	I/O
22	IDSEL0(PAD27)	OUT	57	PCI_CBE0#	I/O	92	IORDY#	IN(O/D)	127	LD8	I/O
23	PAD27	I/O	58	PAD14	I/O	93	GND	-	128	LD0	I/O
24	PAD28	I/O	59	PAD12	I/O	94	LA7	OUT	129	VBATT_IN *2	IN
25	GND	-	60	PAD13	I/O	95	LA14	OUT	130	VBATT_IN *2	IN
26	PAD26	I/O	61	GND	-	96	LA6	OUT	131	VBATT_IN *2	IN
27	GND	-	62	PAD11	I/O	97	LA13	OUT	132	VBATT_IN *2	IN
28	PAD25	I/O	63	GND	-	98	LA5	OUT	133	VBATT_IN *2	IN
29	PAD23	I/O	64	PAD10	I/O	99	LA12	OUT	134	VBATT_IN *2	IN
30	PAD24	I/O	65	PAD8	I/O	100	LA4	OUT	135	VBATT_IN *2	IN
31	PAD22	I/O	66	PAD9	I/O	101	LA11	OUT	136	VBATT_IN *2	IN
32	Reserved	-	67	PAD6	I/O	102	LA3	OUT	137	GND	-
33	PAD21	I/O	68	PAD7	I/O	103	LA10	OUT	138	GND	-
34	Reserved	-	69	PAD4	I/O	104	LA2	OUT	139	GND	-
35	PAD19	I/O	70	PAD5	I/O	105	LA9	OUT	140	GND	-

*1: When the CPU board's power is on, power of +3.3 V (typ.) is supplied to the expansion board.

*2: This is the terminal for the power supply from the expansion board (5.0 - 7.0 V). Power can be supplied from the expansion board to the CPU board.

7.3. Areas over which the expansion board can be expanded

Table 7.3.1 shows the VR5500's memory map

As shown in Table 7.3.1, the expansion board can be expanded to three areas: the PCI space, LDCS1, and LDCS2.

Since the wait number and bus width for each area can be set by configuring the bus controller inside the VRC5477, devices with different access speeds and different bus widths can be used together.

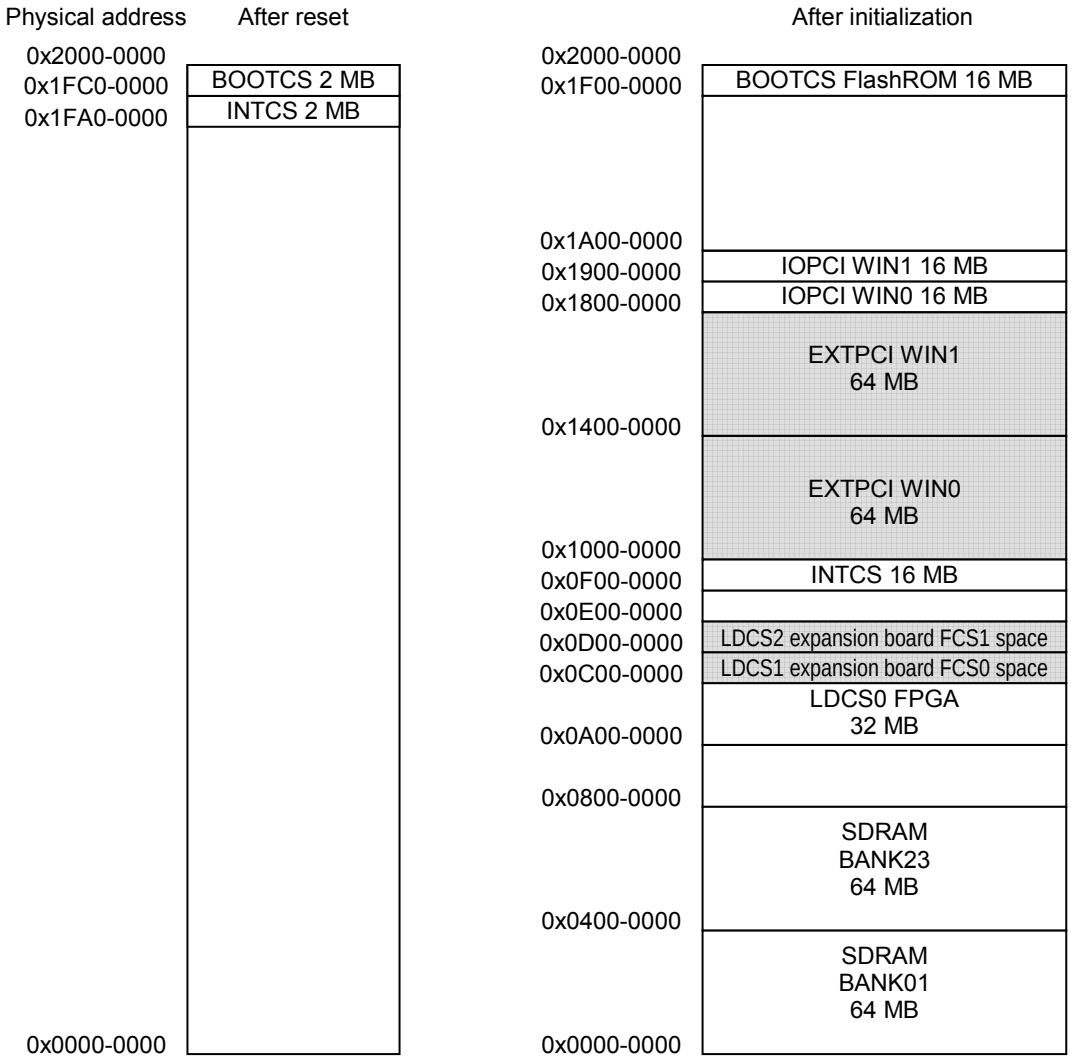


Table 7.3.1: VR5500 memory map

7.4. Power supply to the expansion board

Table 7.4.1 shows the voltage and current of the power supply available from the T-Engine to the expansion board. If the expansion board needs power in excess of this supply, additional steps must be taken to provide a power supply on the expansion board.

The power supply figures shown in Table 7.4.1 are for reference purposes only and are not guaranteed.

Table 7.4.1: Voltage and current of the power supply available to an expansion board

Expansion bus connector signal	Voltage output	Allowable current	Notes
3.3 V	+3.3 V	800 mA	Supplied when the board's power is on

7.5. Interrupt inputs from the expansion board

T-Engine features the following three interrupt input terminals on the expansion bus connector, for use in input of interrupts from the expansion board: PCI_INTA#, PCI_INTB#, and PCI_INTC#. Figure 7.5.1 shows the interrupt terminal structure on the T-Engine expansion bus connector.

Each interrupt terminal in the expansion bus connector recognizes low level interrupts. After the VRC5477 recognizes an interrupt, it issues an interrupt to the VR5500. Interrupts from the VRC5477 to the VR5500 are configured using the VRC5477's register.

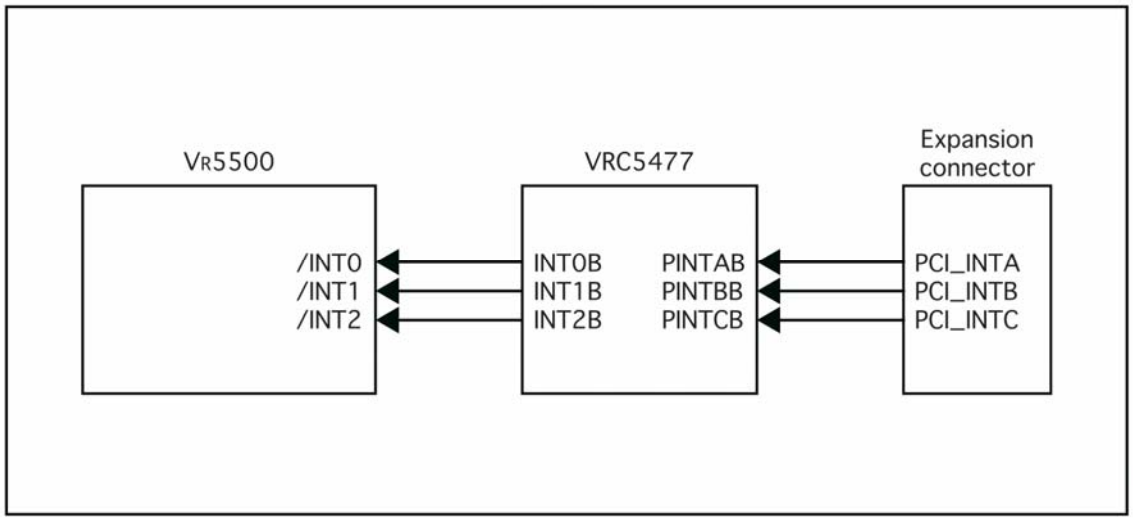


Figure 7.5.1: Interrupt terminal structure on T-Engine expansion bus connector

7.6. Expansion board stacking numbers

Use care with regard to power capacity when stacking multiple expansion boards.

Figure 7.6.1 shows an expansion board stacking structure.

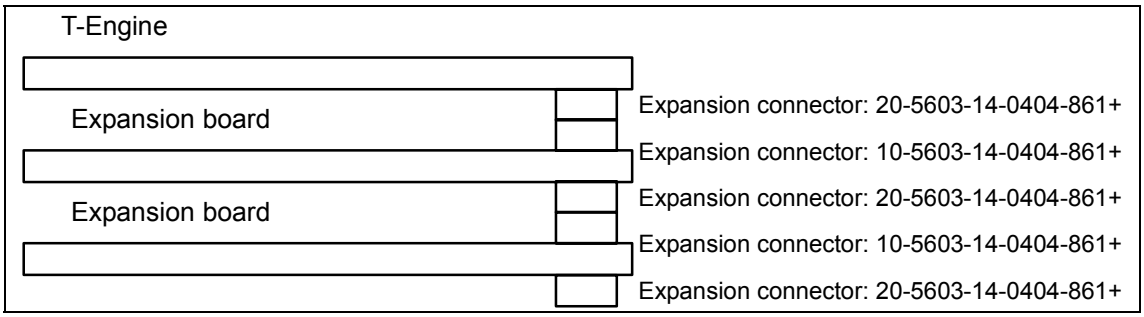


Figure 7.6.1: Expansion board stacking structure

7.7. /WAIT inputs

T-Engine has one IORDY# input terminal on its expansion bus connector, for expansion board /WAIT input. When outputting a WAIT signal from the expansion board, be sure to use open collector output to prevent collision between /WAIT outputs when stacking multiple expansion boards. The IORDY# terminal on the T-Engine side is pulled up at 4.7 kΩ. Figure 7.7.1 shows a structural diagram for the IORDY# terminal in an expansion bus connector.

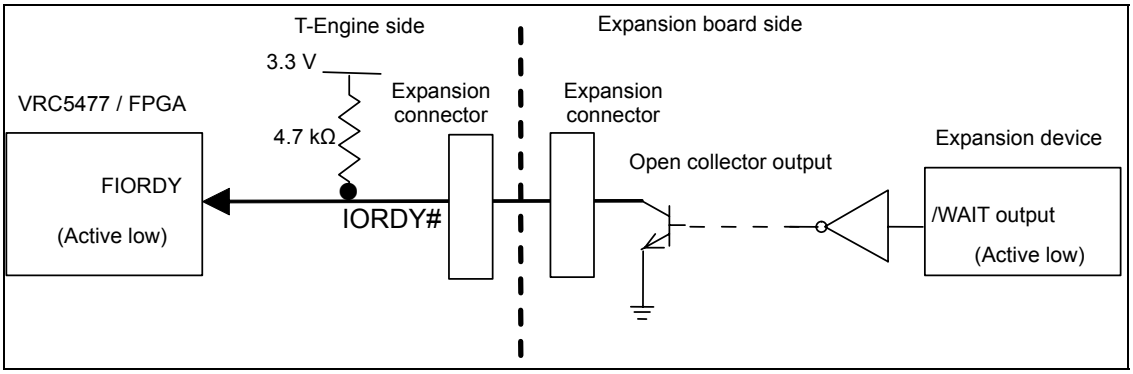


Figure 7.7.1: Structural diagram for IORDY# terminal in expansion bus connector

7.8. AC timing

As shown in Figure 7.8.1, the local bus signals output to the expansion bus connector are output via the bus buffer. For this reason, the bus signal is delayed vs. the timing of the VRC5477 bus. Be sure to take this delay into account when designing an expansion board. Bus timing is shown beginning on the following page.

For details of VRC5477 bus timing, refer to the VRC5477 hardware manual.

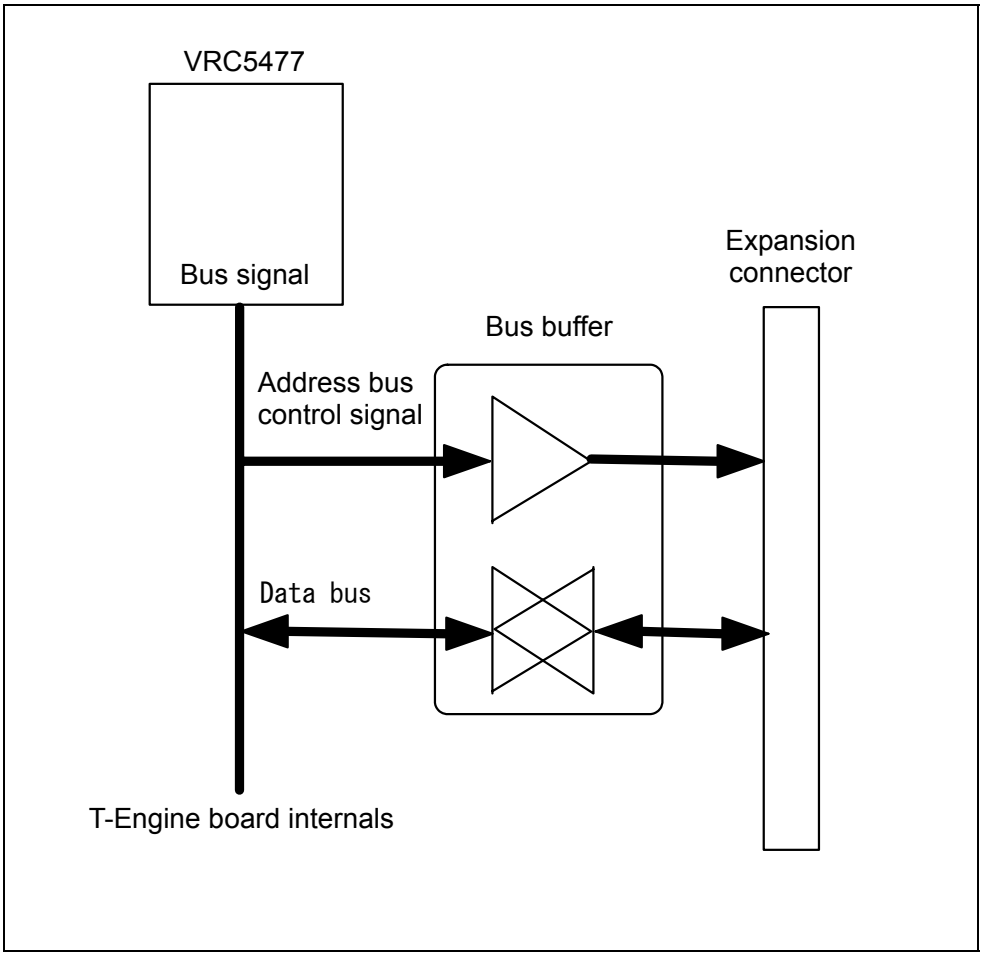
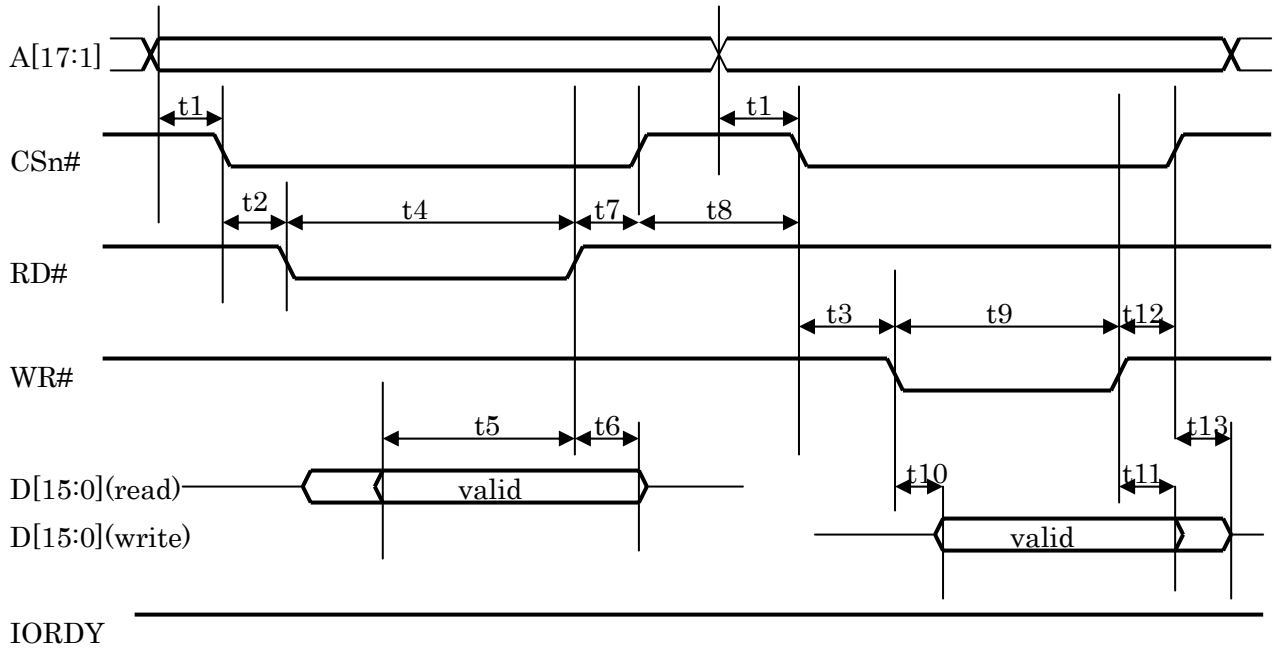
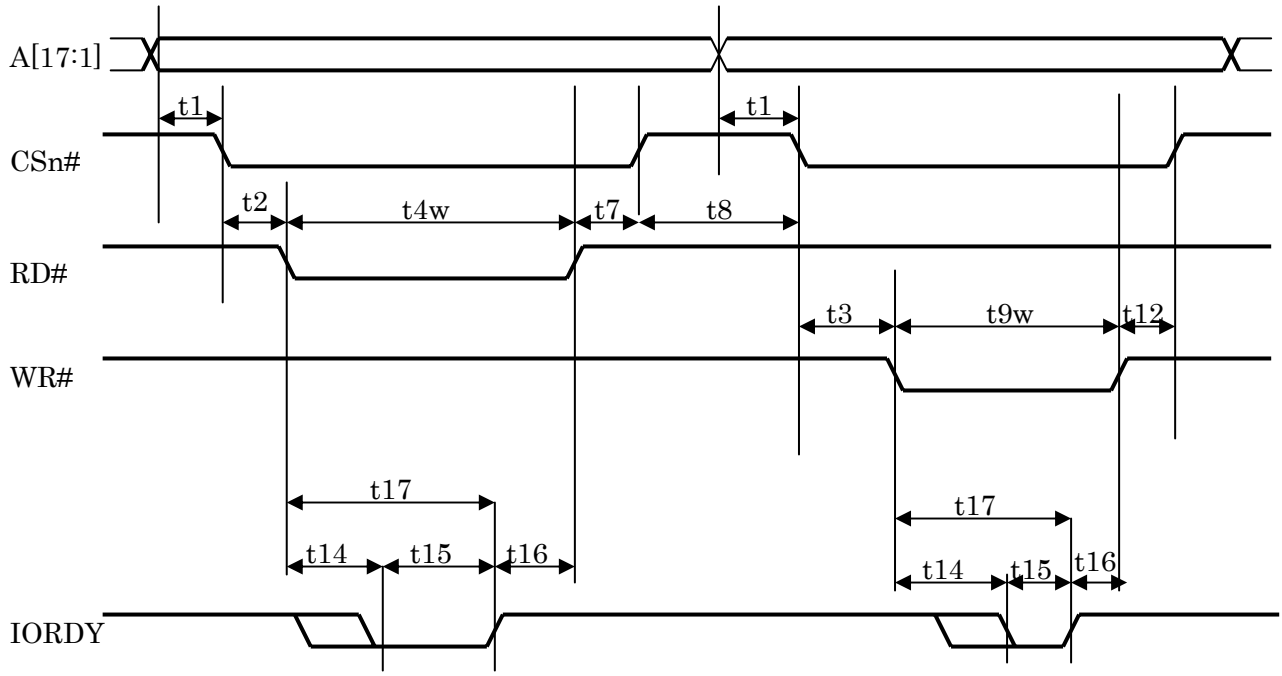


Figure 7.8.1: Expansion bus connector bus buffer structure

• Expansion local bus READ/WRITE timing



• Expansion local bus IORDY timing



- Expansion local bus specifications

Symbol	Description	Min [nS]	Max [nS]
t1	Address valid to CSn# ↓ delay	0	
t2	CSn # ↓ toRD# ↓ delay	0	
t3	CSn # ↓ to WR# ↓ delay	30	
t4	RD# pulse width	160	
t4w	RD# pulse width (with IORDY controlled)	190	
t5	Read data setup	40	
t6	Read data hold	0	30
t7	RD# ↑ to CSn# ↑ delay	0	
t8	CSn# idle width	25	
t9	WR# pulse width	160	
t9w	WR# pulse width (with IORDY controlled)	190	
t10	WR# ↓ to write data valid delay		45
t11	WR# ↑ to write data hold	20	
t12	WR# ↑ to CSn# ↑ delay	25	65
t13	CSn# ↑ to write data disable		25
t14	RD#/WR# ↓ to IORDY ↓ delay	0	120
t15	IORDY pulse width	70	
t16	IORDY ↑ to RD#/WR# ↑ delay	10	
t17	RD#/WR# ↓ to IORDY ↑ delay	190	

Note:

(1) The bus timing delay figure given above is for reference purposes only and is not guaranteed.

■ Chapter 8 VR4131 μT-Engine expansion board design guidelines

This chapter describes design guidelines for expansion boards connecting via the expansion slot on a VR4131 μT-Engine.

The expansion board refers to a board featuring user selected devices etc. and controllable using the VR4131 address bus, data bus, and PCI bus output to the μT-Engine expansion bus connector.

8.1. μT-Engine expansion bus connector specifications

T-Engine connector type implemented: 20-5603-14-0404-861+ (Kyocera Elco)

Compatible connector type: 10-5603-14-0404-861+ (Kyocera Elco)

Figure 8.1 shows the arrangement of the expansion bus connector.

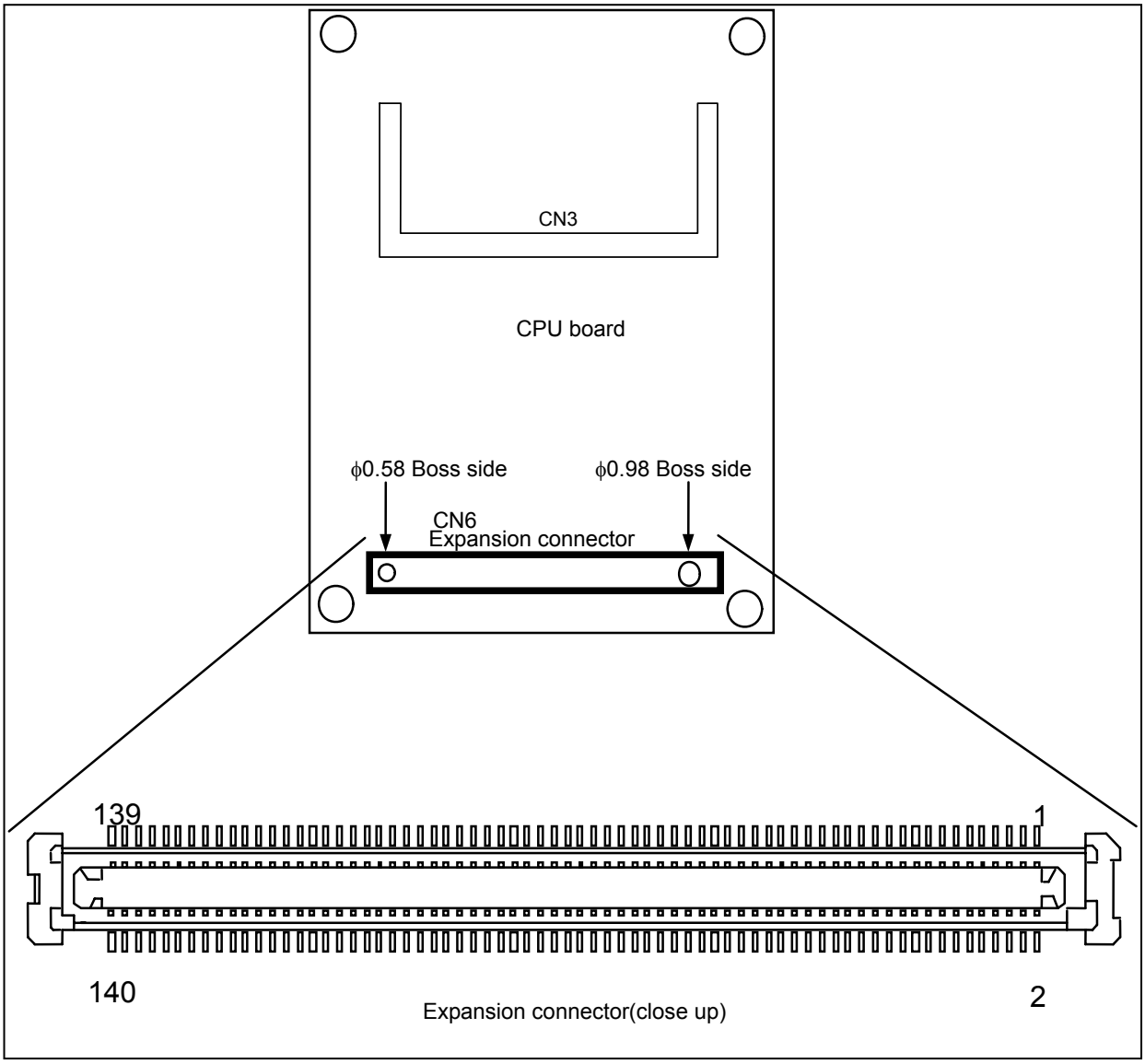


Figure 8.1: Expansion bus connector arrangement

8.2. Expansion bus connector signal arrangement

Table 8.2 shows the arrangement of expansion slot signals.

Both PCI bus and local bus signals are used. The electrical power level is 3.3 V.

Table 8.2: Expansion slot signal arrangement

Pin No.	Signal	I/O	Pin No.	Signal	I/O	Pin No.	Signal	I/O	Pin No.	Signal	I/O
1	GND	-	36	AD20	I/O	71	AD2	I/O	106	A1	OUT
2	PCLK2	OUT	37	GND	-	72	AD3	I/O	107	A8	OUT
3	GND	-	38	AD18	I/O	73	GND	-	108	Reserved	-
4	PCLK1	OUT	39	GND	-	74	AD1	I/O	109	Reserved	-
5	GND	-	40	AD17	I/O	75	GND	-	110	WR#	OUT
6	PCLK0	OUT	41	CBE3#	I/O	76	AD0	I/O	111	GND	-
7	REQ2#	IN	42	AD16	I/O	77	PCIRST#	OUT	112	RD#	OUT
8	VCCIO (3.3V) *1	OUT	43	CBE2#	I/O	78	LOBAT#	IN (O/D)	113	D15	I/O
9	REQ1#	IN	44	STOP#	I/O	79	MPOWER	OUT	114	D7	I/O
10	VCCIO (3.3V) *1	OUT	45	LOCK#	I/O	80	INTA#	IN (O/D)	115	D14	I/O
11	REQ0#	IN	46	PERR#	I/O	81	WAKEUP#	IN (O/D)	116	D6	I/O
12	GNT2#	OUT	47	IRDY#	I/O	82	INTB#	IN (O/D)	117	D13	I/O
13	GND	-	48	TRDY#	I/O	83	Reserved	-	118	D5	I/O
14	GNT1#	OUT	49	GND	-	84	INTC#	IN (O/D)	119	D12	I/O
15	GND	-	50	FRAME#	I/O	85	Reserved	-	120	D4	I/O
16	GNT0#	OUT	51	GND	-	86	INT0#	IN (O/D)	121	D11	I/O
17	AD31	I/O	52	DEVSEL#	I/O	87	A17	OUT	122	D3	I/O
18	IDSEL2 (AD14)	OUT	53	PAR	I/O	88	CS1#	OUT	123	D10	I/O
19	AD30	I/O	54	SERR#	IN(O/D)	89	A16	OUT	124	D2	I/O
20	IDSEL1 (AD13)	OUT	55	CBE1#	I/O	90	CS0#	OUT	125	D9	I/O
21	AD29	I/O	56	AD15	I/O	91	LA15	OUT	126	D1	I/O
22	IDSEL0 (AD12)	OUT	57	CBE0#	I/O	92	IORDY#	IN (O/D)	127	D8	I/O
23	AD27	I/O	58	AD14	I/O	93	GND	-	128	D0	I/O
24	AD28	I/O	59	AD12	I/O	94	A7	OUT	129	VBATT *2	IN
25	GND	-	60	AD13	I/O	95	A14	OUT	130	VBATT *2	IN
26	PAD26	I/O	61	GND	-	96	A6	OUT	131	VBATT *2	IN
27	GND	-	62	AD11	I/O	97	A13	OUT	132	VBATT *2	IN
28	AD25	I/O	63	GND	-	98	A5	OUT	133	VBATT *2	IN
29	AD23	I/O	64	AD10	I/O	99	A12	OUT	134	VBATT *2	IN
30	AD24	I/O	65	AD8	I/O	100	A4	OUT	135	VBATT *2	IN
31	AD22	I/O	66	AD9	I/O	101	A11	OUT	136	VBATT *2	IN
32	Reserved	-	67	AD6	I/O	102	A3	OUT	137	GND	-
33	AD21	I/O	68	AD7	I/O	103	A10	OUT	138	GND	-
34	Reserved	-	69	AD4	I/O	104	A2	OUT	139	GND	-
35	AD19	I/O	70	AD5	I/O	105	A9	OUT	140	GND	-

*1: When the CPU board's power is on, power of +3.3 V (typ.) is supplied to the expansion board.

*2: This is the terminal for the power supply from the expansion board (+3.5 - 9.0 V). Power can be supplied from the expansion board to the CPU board.

8.3. Areas over which the expansion board can be expanded

Table 8.3.1 shows the VR4131's memory map

As shown in Table 8.3.1, the expansion board can be expanded to three areas: the PCI spaces (WIN#1 and WIN#0) and IOCS1.

Since the wait number and bus width for each area can be set by configuring the bus controller inside the VR4131, devices with different access speeds and different bus widths can be used together.

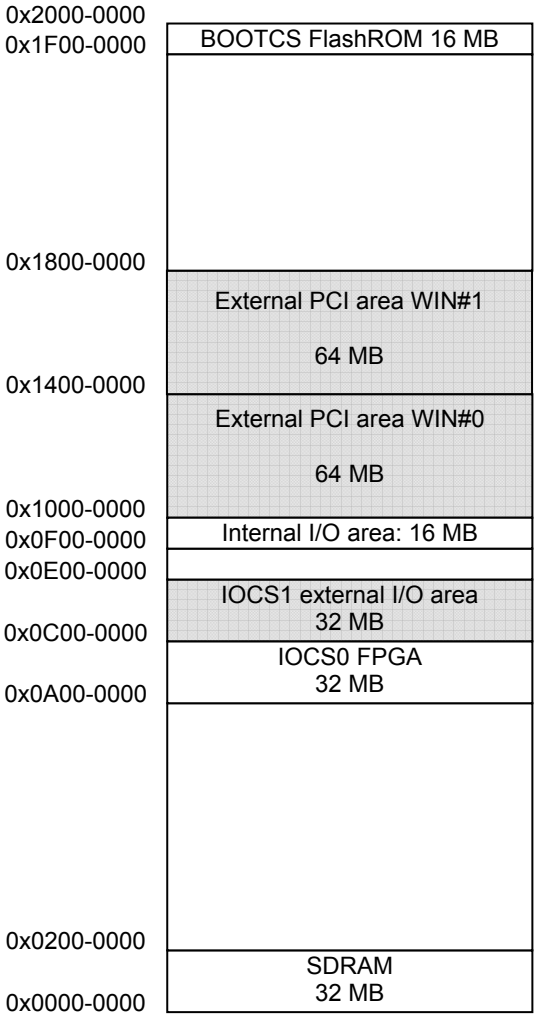


Table 8.3.1: VR4131 memory map

8.4. Power supply to the expansion board

Table 8.4.1 shows the voltage and current of the power supply available from the μT-Engine to the expansion board. If the expansion board needs power in excess of this supply, additional steps must be taken to provide a power supply on the expansion board.

The power supply figures shown in Table 8.4.1 are for reference purposes only and are not guaranteed.

Table 8.4.1: Voltage and current of the power supply available to an expansion board

Expansion bus connector signal	Voltage output	Allowable current	Notes
VCCIO	+3.3 V	500 mA	Supplied when the board's power is on

8.5. Interrupt inputs from the expansion board

In addition to one local bus INT0# interrupt input terminal, μT-Engine features the following three PCI bus interrupt input terminals on the expansion bus connector: INTA#, INTB#, and INTC#. All four of these terminals are for use in input of interrupts from the expansion board. Figure 8.5.1 shows the interrupt terminal structure on the μT-Engine expansion bus connector.

Each interrupt terminal in the expansion bus connector recognizes low level interrupts.

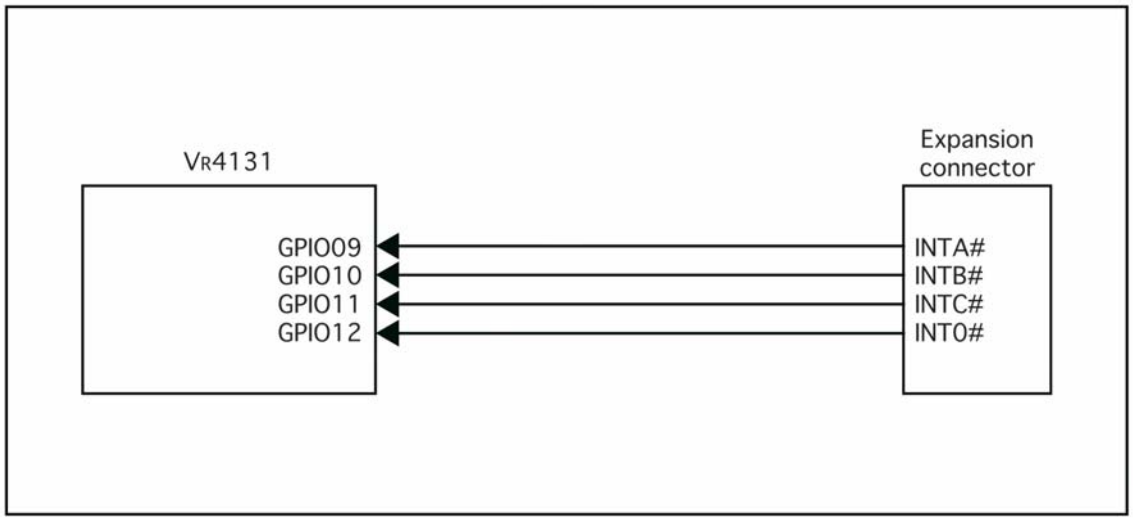


Figure 8.5.1: Interrupt terminal structure on μT-Engine expansion bus connector

8.6. Expansion board stacking numbers

Use care with regard to power capacity when stacking multiple expansion boards.

Figure 8.6.1 shows an expansion board stacking structure.。

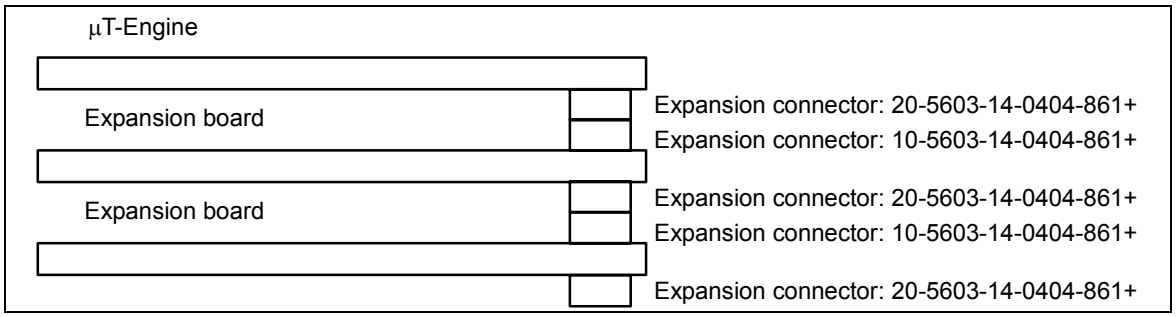


Figure 8.6.1: Expansion board stacking structure

8.7. /WAIT inputs

μT-Engine has one IORDY# input terminal on its expansion bus connector, for expansion board /WAIT input. When outputting a WAIT signal from the expansion board, be sure to use open collector output to prevent collision between /WAIT outputs when stacking multiple expansion boards. The IORDY# terminal on the μT-Engine side is pulled up at 4.7 kΩ. Figure 8.7.1 shows a structural diagram for the IORDY# terminal in an expansion bus connector.

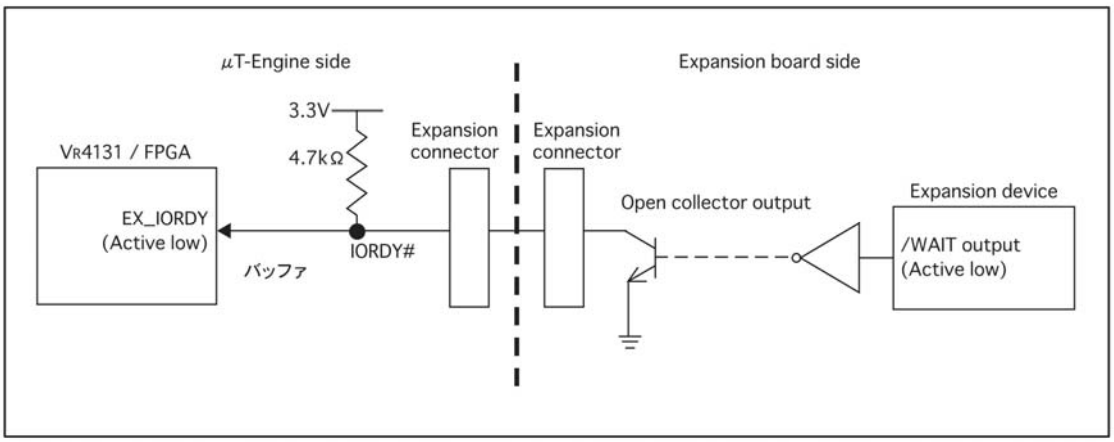


Figure 8.7.1: Structural diagram for IORDY# terminal in expansion bus connector

8.8. AC timing

As shown in Figure 8.8.1, the local bus signals output to the expansion bus connector are output via the bus buffer. For this reason, the bus signal is delayed vs. the timing of the VR4131 bus. Be sure to take this delay into account when designing an expansion board. Bus timing is shown beginning on the following page.

For details of VR4131 bus timing, refer to the VR4131 user's manual.

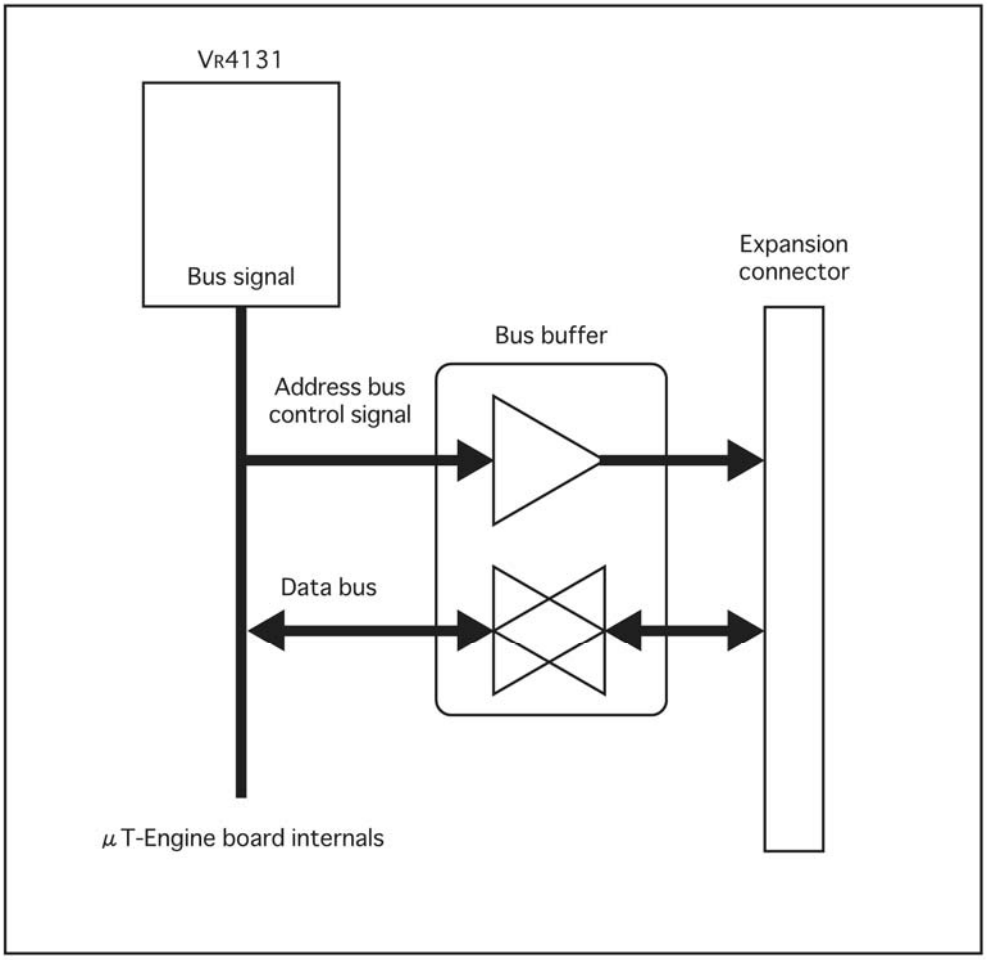
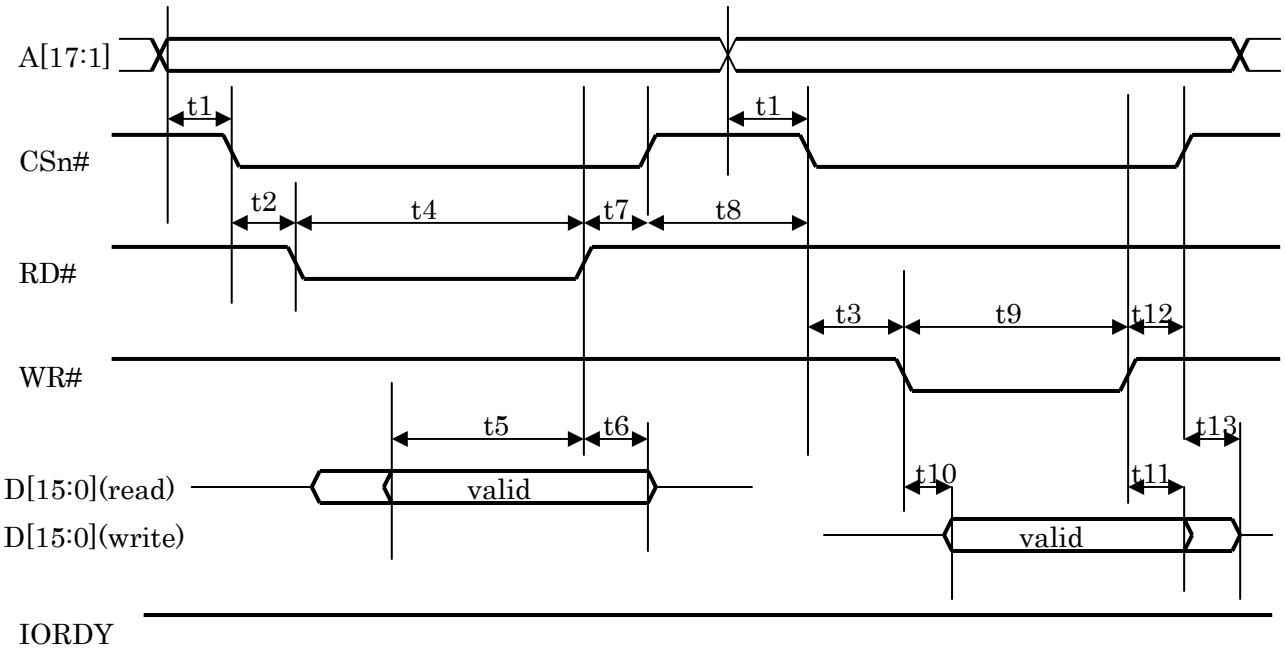
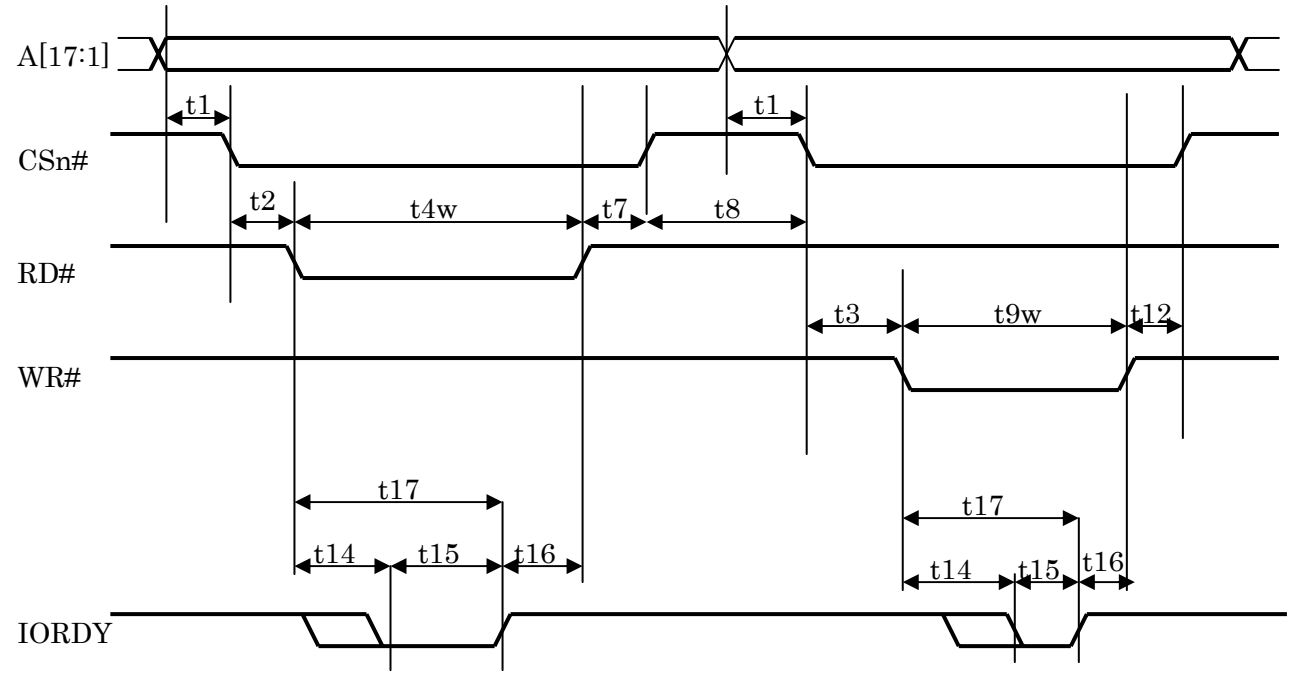


Figure 8.8.1: Expansion bus connector bus buffer structure

• Expansion local bus READ/WRITE timing



• Expansion local bus IORDY timing



• Expansion local bus specifications

Symbol	Description	Min [nS]	Max [nS]
t1	Address valid to CSn# ↓ delay	0	
t2	CSn # ↓ toRD# ↓ delay	0	
t3	CSn # ↓ to WR# ↓ delay	30	
t4	RD# pulse width	160	
t4w	RD# pulse width (with IORDY controlled)	190	
t5	Read data setup	40	
t6	Read data hold	0	30
t7	RD# ↑ to CSn# ↑ delay	0	
t8	CSn# idle width	25	
t9	WR# pulse width	160	
t9w	WR# pulse width (with IORDY controlled)	190	
t10	WR# ↓ to write data valid delay		45
t11	WR# ↑ to write data hold	20	
t12	WR# ↑ to CSn# ↑ delay	25	65
t13	CSn# ↑ to write data disable		25
t14	RD#/WR# ↓ to IORDY ↓ delay	0	120
t15	IORDY pulse width	70	
t16	IORDY ↑ to RD#/WR# ↑ delay	10	
t17	RD#/WR# ↓ to IORDY ↑ delay	190	

Note:

(1) The bus timing delay figure given above is for reference purposes only and is not guaranteed.

■ Chapter 9 V850E/MA3 μT-Engine expansion board design guidelines

This chapter describes design guidelines for expansion boards connecting via the expansion slot on a V850E/MA3 μT-Engine.

The expansion board refers to a board featuring user selected devices etc. and controllable using the V850E/MA3 address bus, data bus, and control signals (start-stop synchronization) or serial signals output to the μT-Engine expansion bus connector.

9.1. μT-Engine expansion bus connector specifications

T-Engine connector type implemented: 20-5603-14-0102-861+ (Kyocera Elco)

Compatible connector type: 10-5603-14-0102-861+ (Kyocera Elco)

Figure 9.1 shows the arrangement of the expansion bus connector.

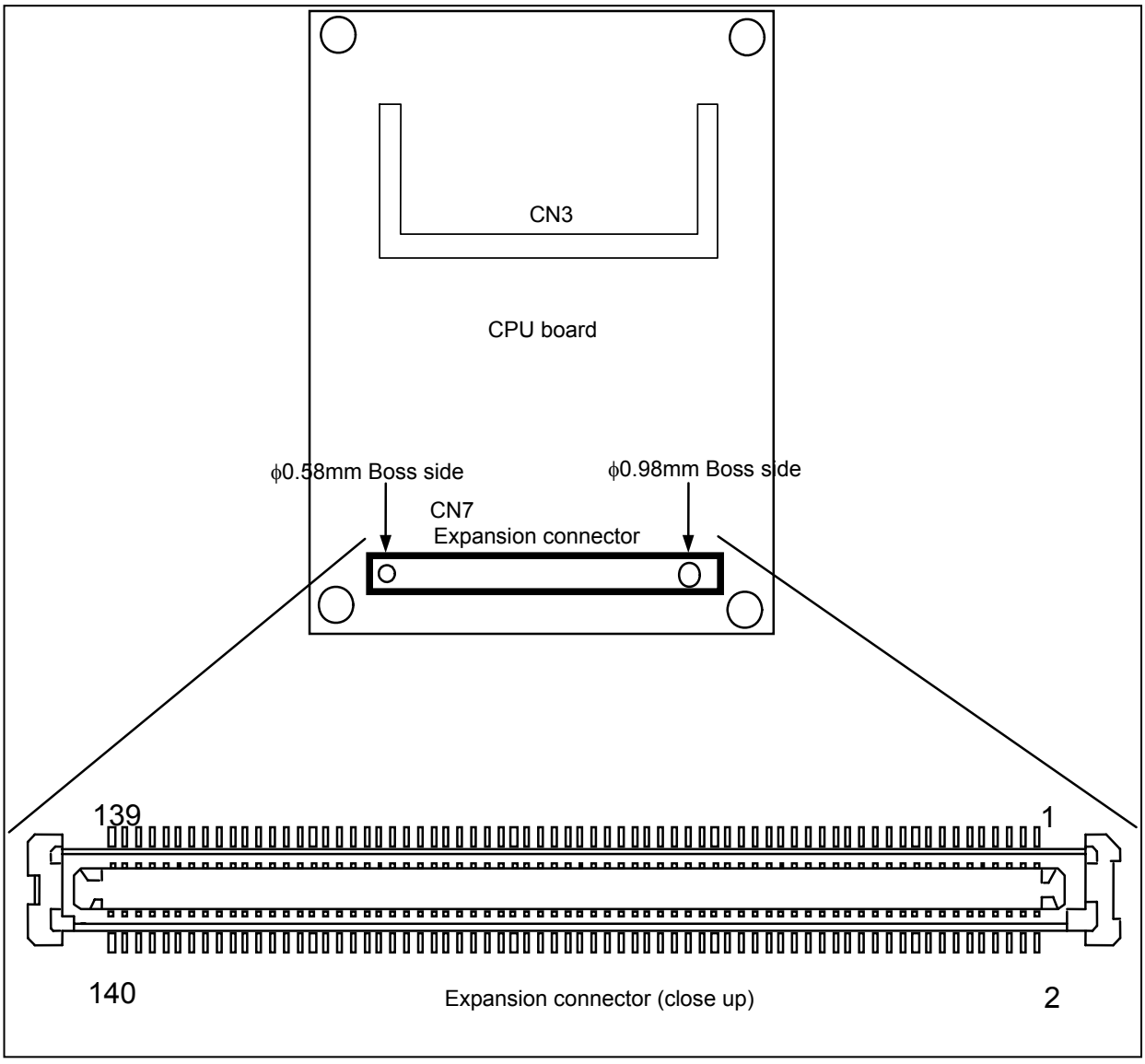


Figure 9.1: Expansion bus connector arrangement

9.2. Expansion bus connector signal arrangement

Table 9.2 shows the arrangement of expansion slot signals.

Local bus signals are used. The electrical power level is 3.3 V.

Table 9.2: Expansion slot signal arrangement

Pin No.	Signal	I/O	Pin No.	Signal	I/O	Pin No.	Signal	I/O	Pin No.	Signal	I/O
1	ANo0	OUT	36	PBD1	I/O	71	A24	OUT	106	ANi6	IN
2	ANo1	OUT	37	PBD2	I/O	72	A25	OUT	107	ANi7	IN
3	MODE0	IN	38	PCT6	I/O	73	Pull-Up	-	108	SCK0	OUT
4	MODE1	IN	39	GND	-	74	EXTCS3-	OUT	109	GND	-
5	AD0	I/O	40	GND	-	75	EXTCS0-	OUT	110	GND	-
6	AD1	I/O	41	EXTBCLK	OUT	76	EXTTXD1-	OUT	111	Pull-Up	-
7	AD2	I/O	42	GND	-	77	EXTRXD1-	IN	112	Pull-Up	-
8	AD3	I/O	43	GND	-	78	EXTRTS1-	OUT	113	Pull-Down	-
9	AD4	I/O	44	GND	-	79	GND	-	114	Pull-Up	-
10	AD5	I/O	45	A0	OUT	80	GND	-	115	Pull-Up	-
11	AD6	I/O	46	A1	OUT	81	EXTRD-	OUT	116	RESERVED	-
12	AD7	I/O	47	A2	OUT	82	EXTWAIT-	IN	117	+3.3VSB *1	OUT
13	AD8	I/O	48	A3	OUT	83	EXTLWR-	OUT	118	+3.3VSB *1	OUT
14	AD9	I/O	49	A4	OUT	84	EXTUWR	OUT	119	+3.3VSB *1	OUT
15	AD10	I/O	50	A5	OUT	85	So0	OUT	120	+3.3VSB *1	OUT
16	AD11	I/O	51	A6	OUT	86	Si0.	IN	121	EXTCS5-	OUT
17	AD12	I/O	52	A7	OUT	87	GND	-	122	EXTCTS1-	IN
18	AD13	I/O	53	A8	OUT	88	GND	-	123	N.C.	-
19	AD14	I/O	54	A9	OUT	89	ANi0	IN	124	N.C.	-
20	AD15	I/O	55	A10	OUT	90	ANi1	IN	125	FPRES-	IN
21	GND	-	56	A11	OUT	91	AGND	-	126	ADTRG	IN
22	GND	-	57	A12	OUT	92	IRQ-	IN	127	+3.3V *2	OUT
23	P10	IN	58	A13	OUT	93	NMIIN	IN	128	+3.3V *2	OUT
24	P11	IN	59	A14	OUT	94	RES_IN-	IN	129	+3.3V *2	OUT
25	P12	IN	60	A15	OUT	95	RES_OUT-	OUT	130	+3.3V *2	OUT
26	P13	I/O	61	GND	-	96	AGND	-	131	+3.3V *2	OUT
27	+2.5VSB	OUT	62	GND	-	97	ANi2	IN	132	+3.3V *2	OUT
28	P14	I/O	63	A16	OUT	98	ANi3	IN	133	VBAT-IN *3	IN
29	N.C.	-	64	A17	OUT	99	Pull-Up	-	134	VBAT-IN *3	IN
30	N.C.	-	65	A18	OUT	100	ANi4	IN	135	VBAT-IN *3	IN
31	EXTDRQ-	IN	66	A19	OUT	101	GND	-	136	VBAT-IN *3	IN
32	P15	I/O	67	A20	OUT	102	GND	-	137	GND	-
33	EXTDAK-	OUT	68	A21	OUT	103	TXD3	OUT	138	GND	-
34	PCM2	I/O	69	A22	OUT	104	RXD3	IN	139	GND	-
35	PCM3	I/O	70	A23	OUT	105	ANi5	IN	140	GND	-

*1: A power supply of +3.3 V (typ.) is provided at all times when an AC adapter is connected.

*2: When the CPU board's power is on, power of +3.3 V (typ.) is supplied to the expansion board.

*3: This is the terminal for the power supply from the expansion board (4.8 - 5.6 V). Power can be supplied from the expansion board to the CPU board.

9.3. Areas over which the expansion board can be expanded

Table 9.3.1 shows the V850E/MA3's memory map

As shown in Table 9.3.1, the expansion board can be expanded to the CS5 area.

Since the wait number and bus width for each area can be set by configuring the bus controller inside the V850E/MA3, devices with different access speeds and different bus widths can be used together.

Table9.3.1: V850E/MA3 memory map

On the μT-Engine/V850E-MA3, each device is mapped to the following physical addresses:

(Physical address)		
xFFF_FFFFh	Internal peripheral I/O	
xFFF_F000h	Internal data RAM 32 KB	CS7
xFFF_EFFFh	PLD01, PLD02 register	
xFE0_0000h	(CPU board)	
xFDF_FFFFh	Expansion bus I/F2 (*2)	CS5
xF80_0000h	(reserved)	
xF7F_FFFFh		CS6
xC00_0000h		
xBFF_FFFFh	CF Card I/F	CS4
x800_0000h		
x7FF_FFFFh	Expansion bus I/F1 (*1) (reserved)	CS3
x400_0000h		
x3FF_FFFFh	Internal peripheral I/O	
x3FF_0000h	Internal data RAM area (mirror)	
x3FE_FFFFh		
x280_0000h		
x27F_FFFFh	SDRAM (8 MB)	CS1
x080_0000h		
x07F_FFFFh	Flash memory (1 MB) Expansion board	
x020_0000h		
x01F_FFFFh		CS0
x010_0000h		
x00F_FFFFh	On board Rom area	
x000_0000h	(512 KB)	

[Overall μT-Engine/V850E-MA3 map]

*1: Expansion bus I/F1 is the area used by devices on the expansion board (LAN, PLD03, USB)

*2: Expansion bus I/F2 is reserved for expansion board 2.

Detailed map

CS	Block	Bus width	Address	Device	Comments
CS0	Block0	16bit	0x000_0000h ~ 0x007_FFFFh	On board (512 KB)	CPU
	Block0	16bit	0x008_0000h ~ 0x01F_FFFFh		
	Block1, 2, 3	16bit	0x020_0000h ~ 0x07F_FFFFh	Flash memory (1 MB)	Expansion board
CS1	—	16bit	0x080_0000h ~ 0x27F_FFFFh	SDRAM (8 MB)	CPU board
	—	16bit	0x280_0000h ~ 0x3FE_FFFFh		
	—	8/16bit	0x3FF_0000h ~ 0x3FF_FFFFh	Internal peripheral I/O/internal data RAM area (mirror)	CPU
CS3	—	16bit	0x400_0000h ~ 0x43F_FFFFh	USB controller uPD720122	Expansion board
	—	16bit	0x440_0000h ~ 0x47F_FFFFh	LAN controller LAN91C111	Expansion board
	—	16bit	0x480_0000h ~ 0x4BF_FFFFh	PLD03 register	Expansion board
	—	16bit	0x4C0_0000h ~ 0x7FF_FFFFh		
CS4	—	16bit	0x800_0000h ~ 0xBFF_FFFFh	Compact Flash (CF)	CPU board
CS6	—	16bit	0xC00_0000h ~ 0xF7F_FFFFh		
CS5	Block4, 5, 6	16bit	0xF80_0000h ~ 0xFDF_FFFFh	Expansion bus I/F2	Expansion board 2 (reserved)
CS7	Block7	16bit	0xFE0_0000h ~ 0xFFE_FFFFh	PLD01, PLD02 register	CPU board
	Block7	16bit	0xFFF_0000h ~ 0xFFF_EFFFh	On-board data RAM (32 KB)	CPU
	Block7	8/16bit	0xFFF_F000h ~ 0xFFF_FFFFh	Internal peripheral I/O	CPU

[Detailed μT-Engine/V850E-MA3 map]

9.4. Power supply to the expansion board

Table 9.4.1 shows the voltage and current of the power supply available from the μT-Engine to the expansion board. If the expansion board needs power in excess of this supply, additional steps must be taken to provide a power supply on the expansion board.

The power supply figures shown in Table 9.4.1 are for reference purposes only and are not guaranteed.

Table 9.4.1: Voltage and current of the power supply available to an expansion board

Expansion bus connector signal	Voltage output	Allowable current	Notes
+3.3 VSB	+3.3 V	500 mA	Supplied when an AC adapter is connected
+3.3 V	+3.3 V		Supplied when the board's power is on

* An allowable current of up to 500 mA for both + 3.3VSB and + 3.3V may be used.

9.5. Interrupt inputs from the expansion board

μT-Engine features two interrupt input terminals on the expansion bus connector for use in input of interrupts from the expansion board. In addition, the attached LAN and USB expansion board uses P10 and P11 for USB and LAN interrupts. Figure 9.5.1 shows the interrupt terminal structure on the μT-Engine expansion bus connector.

Each interrupt terminal in the expansion bus connector recognizes low level interrupts.

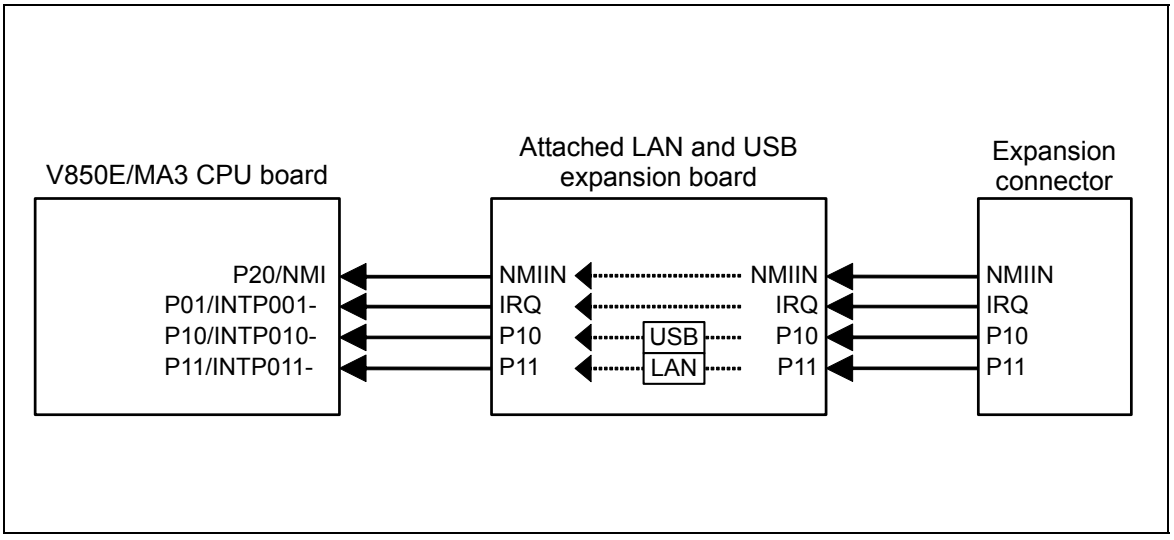


Figure 9.5.1: Interrupt terminal structure on μT-Engine expansion bus connector

Note 1: P10/INTP010- and P11/INTP011- cannot be used by other expansion boards, because they are used by the attached expansion boards.

Note 2: The active level for each interrupt is shown below. For details, see the μT-Engine hardware manual.

P20/NMI: Rising edge

P01/INTP001-: Low level

P10/INTP010-: Low level

P11/INTP011-: Rising edge

9.6. Expansion board stacking numbers

Use care with regard to power capacity when stacking multiple expansion boards.

Figure 9.6.1 shows an expansion board stacking structure.

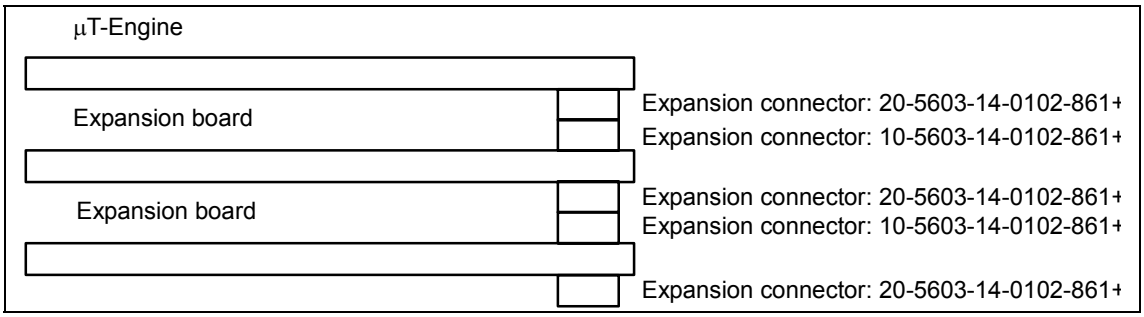


Figure 9.6.1: Expansion board stacking structure

9.7. /WAIT inputs

μT-Engine has one EXTWAIT- input terminal on its expansion bus connector, for expansion board /WAIT input.

The EXTWAIT- signal is used on the attached LAN and USB expansion board. Use EXTWAIT- when needing a wait number equal to or greater than that configurable using the programmable wait settings. Assign a pulse width no smaller than the required EXTRD- and EXTxWR- pulse width.

Figure 9.7.1 shows a structural diagram for the EXTWAIT- terminal in an expansion bus connector.

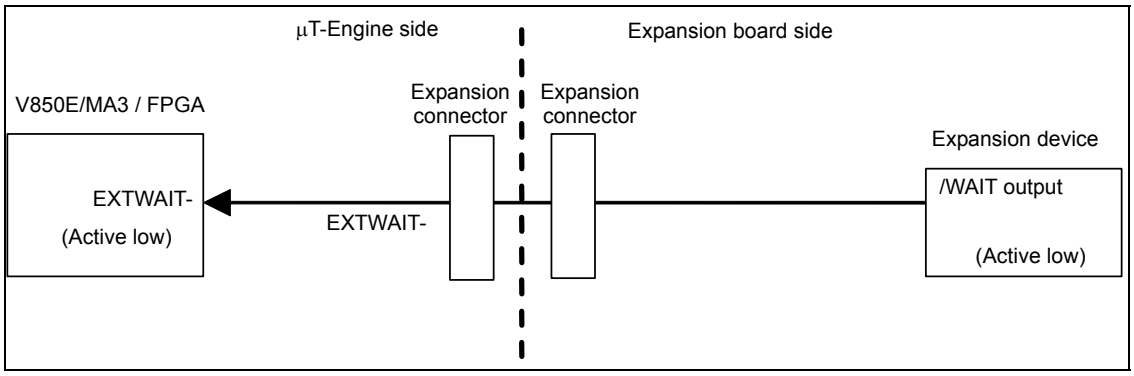


Figure 9.7.1: Structural diagram for EXTWAIT- terminal in expansion bus connector

9.8. AC timing

As shown in Figure 9.8.1, the local bus signals output to the expansion bus connector are output via the bus buffer. For this reason, the bus signal is delayed vs. the timing of the V850A/MA3 bus. Be sure to take this delay into account when designing an expansion board. Bus timing is shown beginning on the following page.

For details of V850A/MA3 bus timing, refer to the V850A/MA3 user's manual.

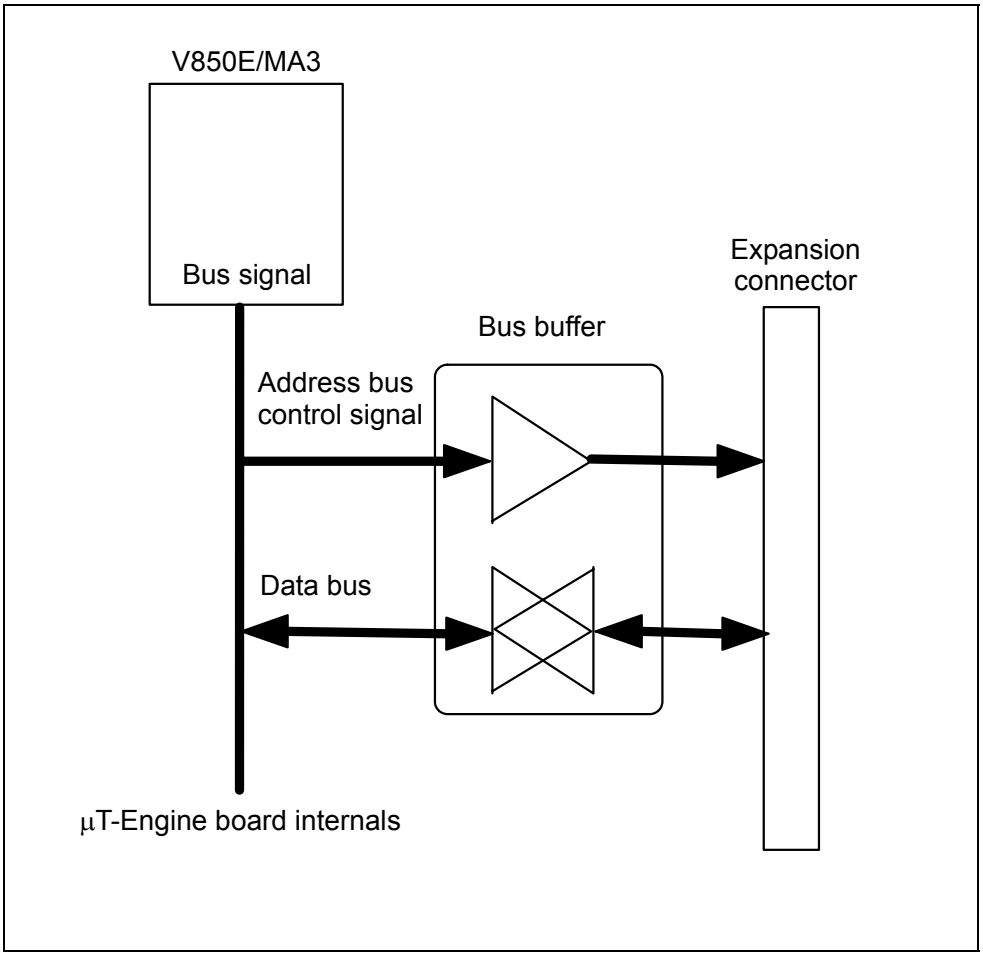


Figure 9.8.1: Expansion bus connector bus buffer structure

Expansion bus DC characteristics

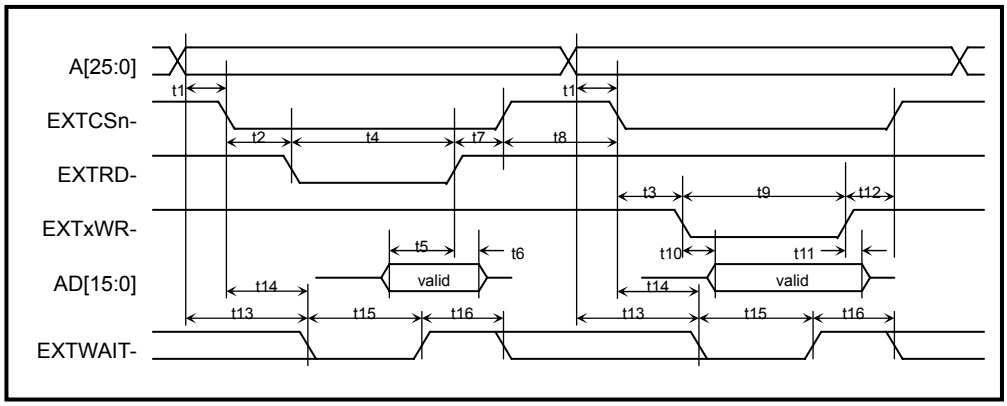
DC characteristics of the expansion bus are shown below:

Item	Symbol	Conditions	MIN	TYP	MAX	Units
High level input voltage	V_{IH}		2.0		3.6	V
Low level input voltage	V_{IL}		0		0.8	V
High level output voltage	V_{OH}	I_{OH} =	2.8			V
		I_{OH} = -1mA	2.3			V
Low level output voltage	V_{OL}	I_{OL} = 3mA			0.4	V
High level input leakage current	I_{LIH}	V_I=3.3V			10	μA
Low level input leakage current	I_{LIL}	V_I=0V			-10	μA

Note: Not including EXTRXD1-, EXTTXD1-, EXTCTS1-, or EXTRTS1-. These signals are RS232C compliant.

Expansion bus AC characteristics

AC characteristics of the expansion bus are shown below:



[Expansion bus timing diagram]

Symbol	Description	Min(nS)	Max(nS)
t1	Address valid to EXTCSn- ↓ delay	0	15
t2	EXTCSn-↓ to EXTRD-↓ delay(*2)	(0.5+WAS) x 25 - 6	
t3	EXTCSn-↓ to EXTxWR-↓ delay (*1)(*2)	(0.5+WAS) x 25 - 6	
t4	EXTRD- pulse width (*3)	(1.5+W) x 25 -4	
t5	Read data setup	41	
t6	Read data hold	0	
t7	EXTRD-↑ to EXTCSn-↑ delay	0	
t8	ETXCSn- idle width (*5)	i×25	
t9	EXTxWR- pulse width (*1) (*3)	(1+W) x 25 - 4	
t10	EXTxWR-↓ to write data valid delay (*1)		3.5
t11	EXTxWR-↑ to write data hold (*1) (*5)	(0.5+i) x 25 - 19	
t12	EXTxWR-↑ to EXTCSn-↑ delay (*1)	8.5	
t13	Address to EXTWAIT-↓ delay (*2)		(1+WAS) x 25 - 39
t14	EXTCS5- to EXTWAIT-↓ delay (*2)		(1+WAS) x 25 - 54
t15	EXTWAIT- Low pulse width	(*6)	
t16	EXTWAIT- High pulse width	21	

Expansion bus: CN7/CPU-board characteristics table]

Symbol	Description	Min(nS)	Max(nS)
t1	Address valid to EXTCS5-↓ delay	0	15
t2	EXTCS5-↓ to EXTRD-↓ delay (*2)	(0.5+WAS) x 25 - 6	
t3	EXTCS5-↓ to EXTxWR-↓ delay (*1) (*2)	(0.5+WAS) x 25 - 6	
t4	CS5 Area : EXTRD- pulse width (*4)	(1.5+W) x 25 -4	
t5	CS5 Area : Read data setup	41	
t6	Read data hold	0	
t7	EXTRD-↑ to EXTCS5-↑ delay	0	
t8	EXTCS5- idle width (*5)	I x 25	
t9	CS5 Area : EXTxWR- pulse width (*1) (*4)	(1+W) x 25 - 4	
t10	EXTxWR-↓ to write data valid delay (*1)		3.5
t11	CS5 Area : EXTxWR-↑ to write data hold (*1)(*5)	(0.5+i) x 25 - 19	
t12	EXTxWR-↑ to EXTCS5-↑ delay (*1)	8.5	
t13	Address to EXTWAIT2-↓ delay (*2)		(1+WAS) x 25 - 49
t14	EXTCS5- to EXTWAIT2-↓ delay (*2)		(1+WAS) x 25 - 64
t15	EXTWAIT2- Low pulse width	(*6)	
t16	EXTWAIT2- High pulse width	21	

[Expansion bus: CN2/expansion board characteristics table]

Notes:

*1: EXTxWR- refers to EXTLWR- and EXTUWR-.

*2: Depends on the value set to the CPU's ASC register (address setup wait number). WAS is the address setup wait number.

*3: Depends on the EXTWAIT- terminal input width and the value set to the CPU's DWC0, 1 register (programmable wait number.) W is the higher of the following: the EXTWAIT- terminal's wait number and the programmable wait number.

*4: Depends on the EXTWAIT2- terminal input width and value set to the CPU's DWC0, 1 register (programmable wait number). W is the higher of the following: the EXTWAIT2- terminal's wait number and the programmable wait number.

*5: Depends on the value set to the CPU's BCC register (idle state number). The letter "i" indicates the idle state number.

*6: Use EXTWAIT- and EXTWAIT2- when a wait equal to or longer than the number that can be set to the programmable wait is needed. Assign a pulse width no smaller than the EXTRD- and EXTxWR- pulse width.

Note:

(1) The bus timing delay figure given above is for reference purposes only and is not guaranteed.

■ Chapter 10 ARM T-Engine expansion board design guidelines

This chapter describes design guidelines for expansion boards connecting via the external expansion port on an ARM T-Engine. The expansion board refers to a board featuring user selected devices etc. and controllable using the ARM address bus, data bus, and control signals output to the T-Engine expansion bus connector.

10.1. T-Engine expansion bus connector specifications

T-Engine, μT-Engine connector type implemented: 2x-5603-14-0303-861+ (Kyocera Elco)

Compatible connector type: 1x-5603-14-0303-861+ (Kyocera Elco; the character in the space denoted by "x" indicates packaging type and may be ignored)

Figure 10.1 shows the arrangement of the expansion bus connector.
(This diagram illustrates the arrangement for standard T-Engine. μT-Engine uses the same arrangement.)

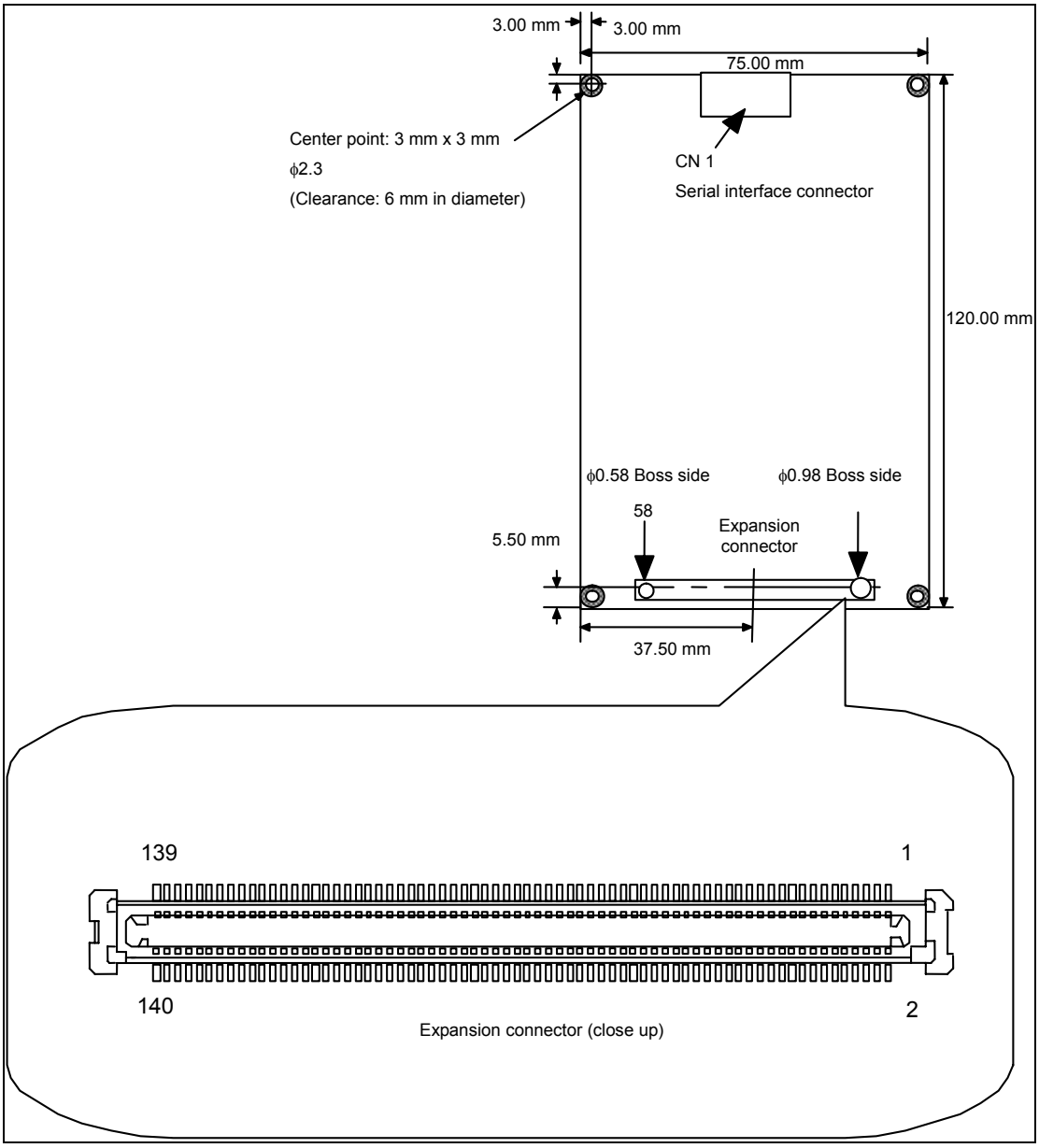


Figure 10.1: Expansion bus connector arrangement (top view)

10.2. Expansion board size

It is recommended that an expansion board have the same size (120 mm x 75 mm or 85 mm x 60 mm) as a T-Engine board.

In principle, do not install any components on side A (the CPU board side) of the expansion board.

Be sure not to install any components greater than 9 mm in height on side B (the expansion LAN board side) of the expansion board. However, for a bottom board on which only a PLUG will be installed, with no expansion board used, components less than 15 mm in height may be installed on side B.

Rules concerning board dimensions are summarized below.

(1) Use a board thickness of 1.6 mm.

(2) Place a hole 2.1 mm in diameter in each of the four corners of the board, for use in installing the board. Center each hole 3.0 mm or 2.5 mm from the edge of the board. Be sure not to install any components or patterns (other than GND) within the area 3.0 mm or 2.5 mm in radius from the center of each hole.

(3) Center the expansion bus connector's boss hole 5.5 mm from the edge of the board. Center the expansion bus connector on the center of the board.

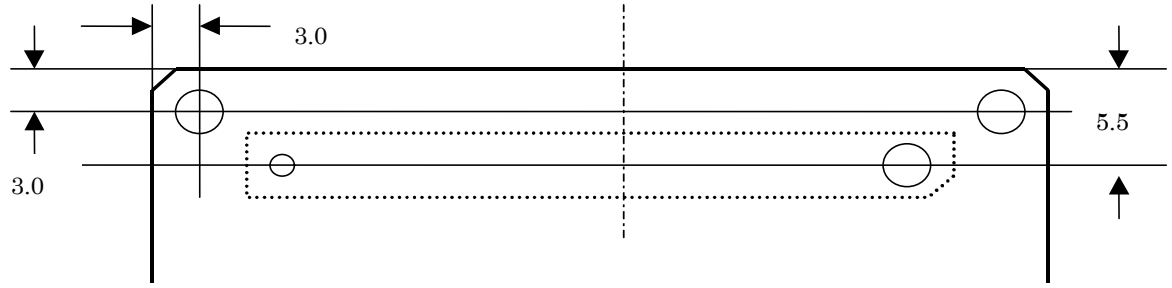


Figure 10.2.1: Dimensions around the expansion bus connector on a standard T-Engine

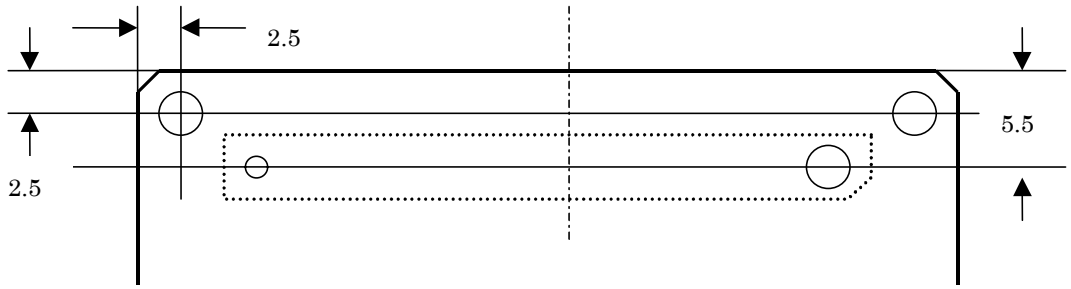
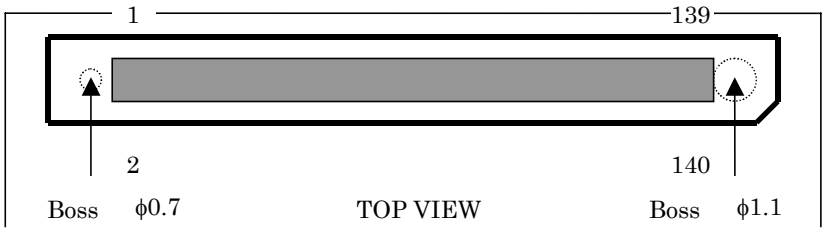


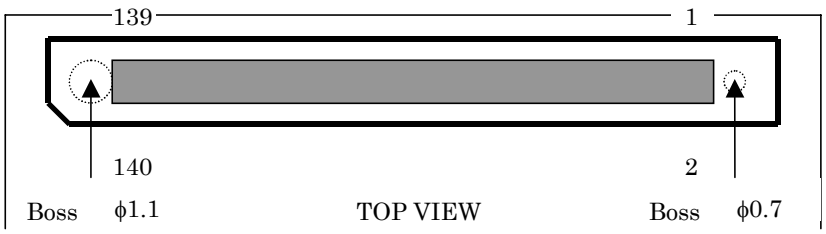
Figure 10.2.2: Dimensions around the expansion bus connector on a μT-Engine

10.3. Direction in which to install the expansion bus connector

Figure 10.3 shows the direction in which to install the expansion bus connector. Use care when designing patterns, because the pin numbers of the connector are the reverse of the pin numbers of the component as designated by the connector manufacturer.



Side A: PLUG



Side B:RECE

Figure 10.3: Direction in which to install expansion bus connector

10.4. Expansion bus connector signal arrangement

Table 10.4 shows the arrangement of expansion slot signals.

Table 10.4: Expansion slot signal arrangement

Pin No.	Signal	I/O	Pin No.	Signal	I/O	Pin No.	Signal	I/O	Pin No.	Signal	I/O
1	EXB_5V **(*1)**	OUT	36	D27	I/O	71	CS2#	OUT	106	RSV11	-
2	EXB_5V	OUT	37	D28	I/O	72	CS3#	OUT	107	GND	-
3	EXB_5V	OUT	38	D29	I/O	73	WE0#	OUT	108	GND	-
4	EXB_5V	OUT	39	D30	I/O	74	R/W **(*2)**	OUT	109	RSV12	-
5	EXB_5V	OUT	40	D31	I/O	75	GND	-	110	RSV13	-
6	EXB_5V	OUT	41	GND	-	76	GND	-	111	RSV14	-
7	D0	I/O	42	GND	-	77	CLK	OUT	112	RSV15	-
8	D1	I/O	43	A0	OUT	78	BE2# **(*3)**	OUT	113	RSV16	-
9	D2	I/O	44	A1	OUT	79	GND	-	114	RSV17	-
10	D3	I/O	45	A2	OUT	80	BE3# **(*3)**	OUT	115	RSV18	-
11	D4	I/O	46	A3	OUT	81	OE#	OUT	116	RSV19	-
12	D5	I/O	47	A4	OUT	82	RESERVED	-	117	RSV20	-
13	D6	I/O	48	A5	OUT	83	BREQ0#	IN	118	BATTERY_SIO **(*5)**	I/O
14	D7	I/O	49	A6	OUT	84	BACK#	OUT	119	RSV22	-
15	D8	I/O	50	A7	OUT	85	BE0# **(*3)**	OUT	120	advise_EME **(*6)**	IN
16	D9	I/O	51	A8	OUT	86	BE1# **(*3)**	OUT	121	GND	-
17	D10	I/O	52	A9	OUT	87	WAIT#	IN	122	GND	-
18	D11	I/O	53	A10	OUT	88	DEOT#	OUT	123	INT	IN
19	D12	I/O	54	A11	OUT	89	DREQ0#	IN	124	WDTOUT	OUT
20	D13	I/O	55	A12	OUT	90	DREQ1#	IN	125	PORST#	OUT
21	D14	I/O	56	A13	OUT	91	DACK0#	OUT	126	RTCK	OUT
22	D15	I/O	57	A14	OUT	92	DACK1#	OUT	127	RESET#	OUT
23	GND	-	58	A15	OUT	93	GND	-	128	TRST#	IN
24	GND	-	59	GND	-	94	GND	-	129	TCK	IN
25	D16	I/O	60	GND	-	95	RSV0 **(*4)**	-	130	TMS	IN
26	D17	I/O	61	A16	OUT	96	RSV1	-	131	TDI	IN
27	D18	I/O	62	A17	OUT	97	RSV2	-	132	TDO	OUT
28	D19	I/O	63	A18	OUT	98	RSV3	-	133	VBAT **(*7)**	IN
29	D20	I/O	64	A19	OUT	99	RSV4	-	134	VBAT	IN
30	D21	I/O	65	A20	OUT	100	RSV5	-	135	VBAT	IN
31	D22	I/O	66	A21	OUT	101	RSV6	-	136	VBAT	IN
32	D23	I/O	67	A22	OUT	102	RSV7	-	137	GND	-
33	D24	I/O	68	A23	OUT	103	RSV8	-	138	GND	-
34	D25	I/O	69	CS0#	OUT	104	RSV9	-	139	GND	-
35	D26	I/O	70	CS1#	OUT	105	RSV10	-	140	GND	-

Shaded areas ☐ denote ARM address bus, data bus, control signals, and serial signals. The electrical power level is 3.3 V.

*1: When using a DipSW or allocated I/O port, power of 5.0 V (typ.) is supplied.

*2: Not connected on many models. Use WE# or 0E# instead.

*3: When using LH7A400 Core, BE is not output during WE# assertion. Note that endian notation varies by model.

*4: Allocation of RSVx notation varies by model. See the user's manual.

*5: This port is provided for use in controlling the battery board. It is connected to the MPU serial port. Since

this is connected in the try state, bidirectional communication is possible using a single line. Be sure to define protocols before use.

*6: The main board's ROM can be removed. (ICE emulation RAM or user ROM can be connected.)

*7: This is intended for use in inputs from the battery board. The main board will run when 3.6 - 5.0 (+5%, -0%) V is input.

10.5. Areas over which the expansion board can be expanded

Table 10.5 shows the ARM memory map (TTM109 Freescale MC9328MX21).

As shown in Table 10.5, the expansion board can be expanded to three areas: CS1, 3, and 5. (The names of these areas differ from those of external expansion ports.) However, since CS1 is not output to the standard ARM CS terminal, it is not compatible with standard optional boards for the ARM bus. Specifically, the TTM109 CS1 cannot be selected in TTZ101-002 (LAN board) CS selection.

Since the wait number and bus width for each area can be set by configuring the bus controller inside the MPU, devices with different access speeds and different bus widths can be used together.

Table 10.5: TTM109 memory map

Area no.	Bus width	MPU space	Space name	Device (usable space)	Notes
CSD0	32bit	h'C0000000 ~ h'C3FFFFFF	SD-RAM area	64 MB MT48V16M16LFxx-75 (Micron)	
CSD1	-	h'C4000000 ~ h'C7FFFFFF	SD-RAM area	Unused	
CS0	32bit	h'C8000000 ~ h'CBFFFFFF	Flash ROM area	16 MB MBM29DL640E90TN (Fujitsu) x 2	Output to external expansion port CS0#
CS1	8bit/ 8,16,32bit	h'CC000000 ~ h'CFFFFFFF	FPGA area + user open/user open	User open address range when selecting "FPGA area + user open": h'CC000000 - CCFFFFFF (16 MB) Memory range when selecting "user open" (64 MB)	Output to external expansion port RSV20 (port no. 117) A Dip SW can be used to select either "FPGA area + user open (8 bit)" or "user open (8, 16, 32 bit)"
CS2	-	h'D0000000 ~ h'D0FFFFFF	-	Not usable	Cannot be used (PinMultiplex)
CS3	8,16,32bit	h'D1000000 ~ h'D1FFFFFF	User open	16 MB	Output to external expansion port CS1#
CS4	Not usable 8bit	h'D2000000 ~ h'D2FFFFFF	Not usable/FPGA area	none/ FPGA	Output to external expansion port CS2# A Dip SW can be used to select either "not usable" or "FPGA area"
CS5	8,16bit/ 8,16,32bit	h'D3000000 ~ h'D3FFFFFF	PC card + user open/user open	User open address range: h'D3400000~h'D3FFFFFF (12 MB)	Output to external expansion port CS3# CS4 cannot be used when using external wait When using a PC card at the same time, caution is required in regard to bit-width changes (since the PC-card driver might change the bit width)

* For the area for which bit width is restricted by the user open setting a setting other than the restricted bit width can be used by changing the bit width using the Chip Select x Upper Control Register as needed.

10.6. Power supply to the expansion board

Table 10.6 shows the voltage and current of the power supply available from the T-Engine to the expansion board. If the expansion board needs power in excess of this supply, additional steps must be taken to provide a power supply on the expansion board. These calculations are based on main-board power consumption of no more than 2 W and AC adapter output of 5.0 V and 2.0 A. The power supply figures shown in Table 10.6 are for reference purposes only and are not guaranteed.

Table 10.6: Voltage and current of the power supply available to an expansion board

Expansion bus connector signal	Voltage output	Allowable current	Notes
EXB 5 V	5.0 V	1400 mA (*1)	When using an AC adapter
EXB 5 V	5.0 V	370 mA (*1)(*2)	When using a battery board

*1: When running the USB host controller using bus power and when using a 5V PC CARD card, deduct the power used.

*2: Calculations are based on a 0.5 A power supply from the battery board (TTZ101-003). This depends on the power consumption balance with the main board. When connecting a power supply other than a battery board to the VBAT terminal, this figure will vary depending on the capacity of the power supply connected.

10.7. Interrupt inputs from the expansion board

T-Engine features an INT7$ (negative logic) interrupt input terminal on the expansion bus connector for use in input of interrupts from the expansion board. (Some models feature multiple interrupt input terminals assigned to their RSV terminals.) Figure 10.7 shows the interrupt terminal structure on the T-Engine expansion bus connector.

Each interrupt terminal in the expansion bus connector recognizes low level interrupts. After an interrupt is recognized, it is converted at the logic level by the interrupt controller in the T-Engine's FPAG and an interrupt is issued to the ARM Core.

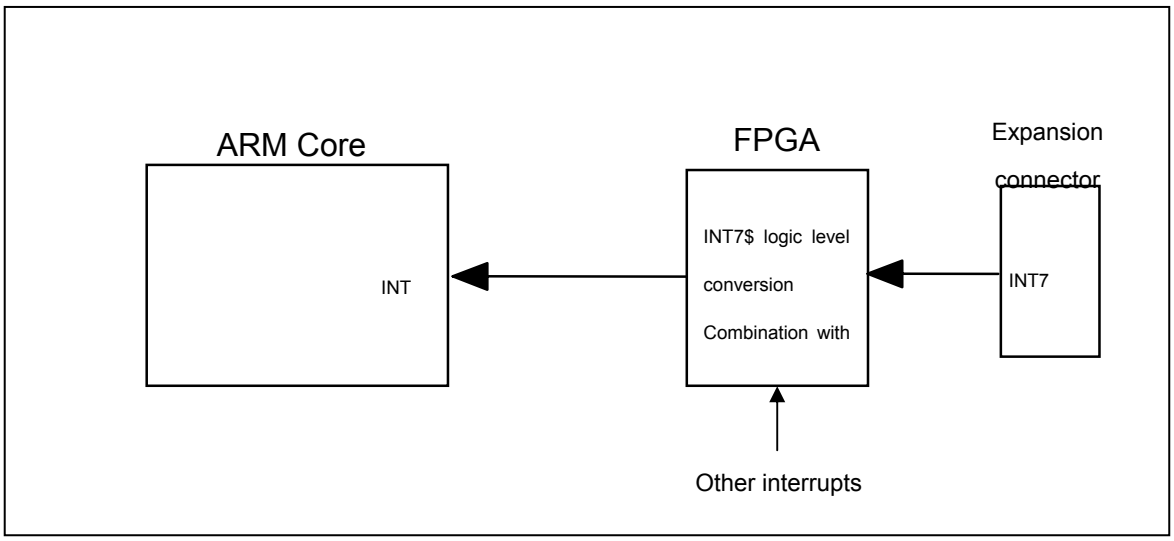


Figure 10.7: Interrupt terminal structure on T-Engine expansion bus connector

Notes:

Methods of connecting INT terminals vary by model. In most cases, these are inverted on the logic level inside the FPGA. The expansion bus connector uses negative logic. There is an interrupt controller inside the FPGA, and an interrupt is combined with others inside the board. Selection and masking of edge interrupts and level interrupts can be conducted.

10.8. Expansion board stacking numbers

Use care with regard to power capacity when stacking multiple expansion boards.

Figure 10.8 shows an expansion board stacking structure.

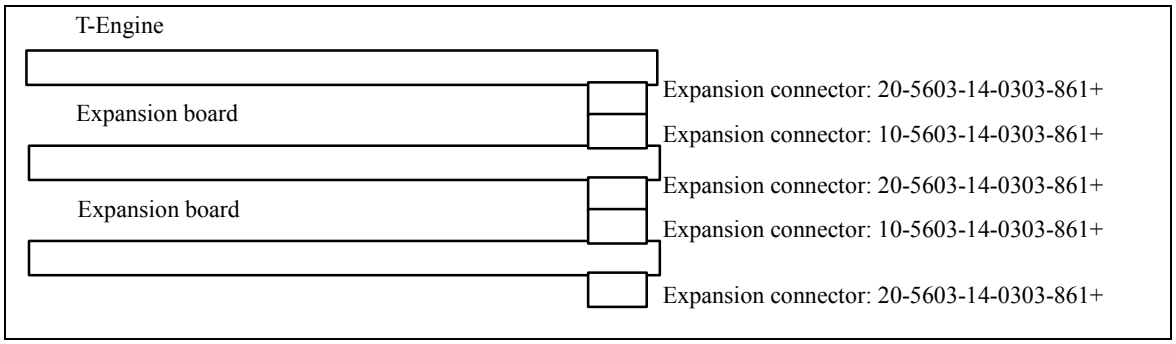


Figure 10.8: Expansion board stacking structure

10.9. EXT_WAIT# inputs

T-Engine has one WAIT input terminal on its expansion bus connector, for expansion board WAIT input. When outputting a WAIT signal from the expansion board, be sure to use open collector output to prevent collision between /WAIT outputs when stacking multiple expansion boards. The EXT_WAIT# terminal on the T-Engine side is pulled up at 1 kΩ. Figure 10.9 shows a structural diagram for the /WAIT terminal in an expansion bus connector.

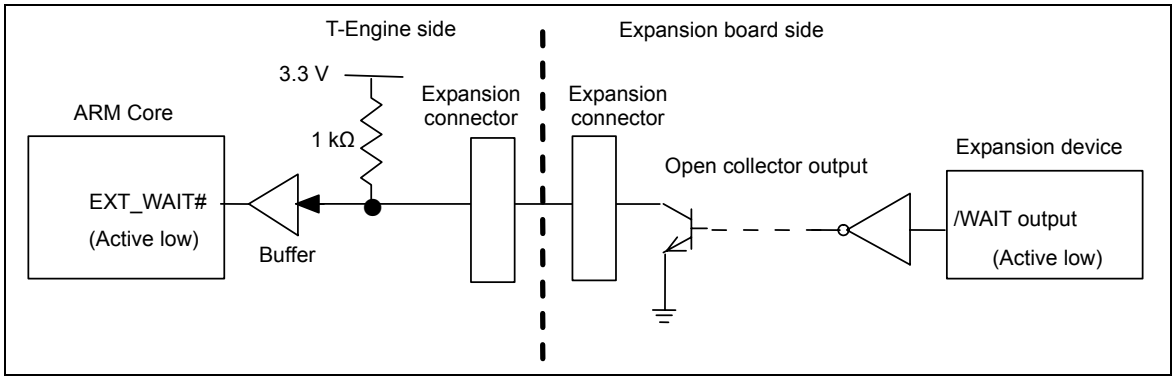


Figure 10.9: Structural diagram for EXT_WAIT# terminal in expansion bus connector

10.10. AC timing

As shown in Figure 10.10, most ARM-bus signals output to the expansion bus connector are output via the bus buffer. For this reason, the bus signal is delayed by approximately 10 nsec vs. the AC timing of the ARM bus. Be sure to take this delay into account when designing an expansion board. Basic ARM bus timing examples (TTM109) are shown on the next page.

For details of ARM bus timing, refer to the respective ARM Core hardware manuals.

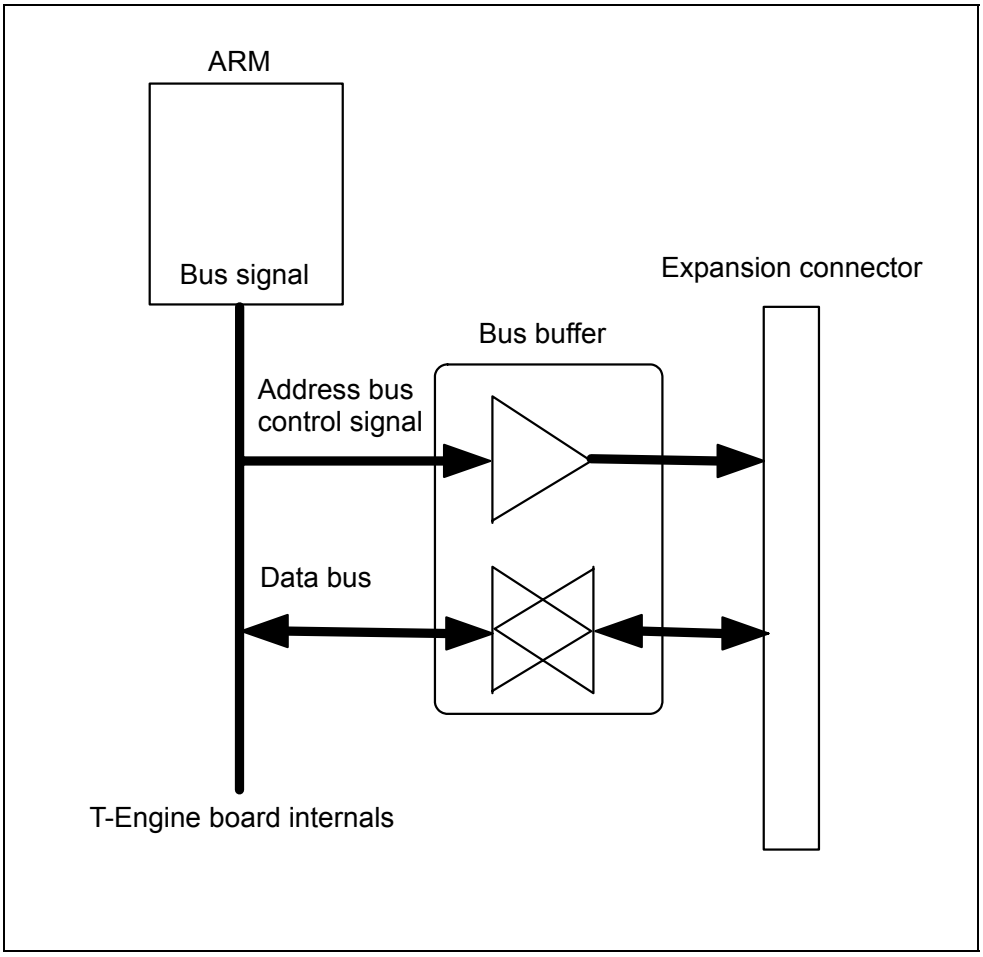


Figure 10.10: Expansion bus connector bus buffer structure

Note:

(1) The bus timing delay figure given above is for reference purposes only and is not guaranteed.

AC timing

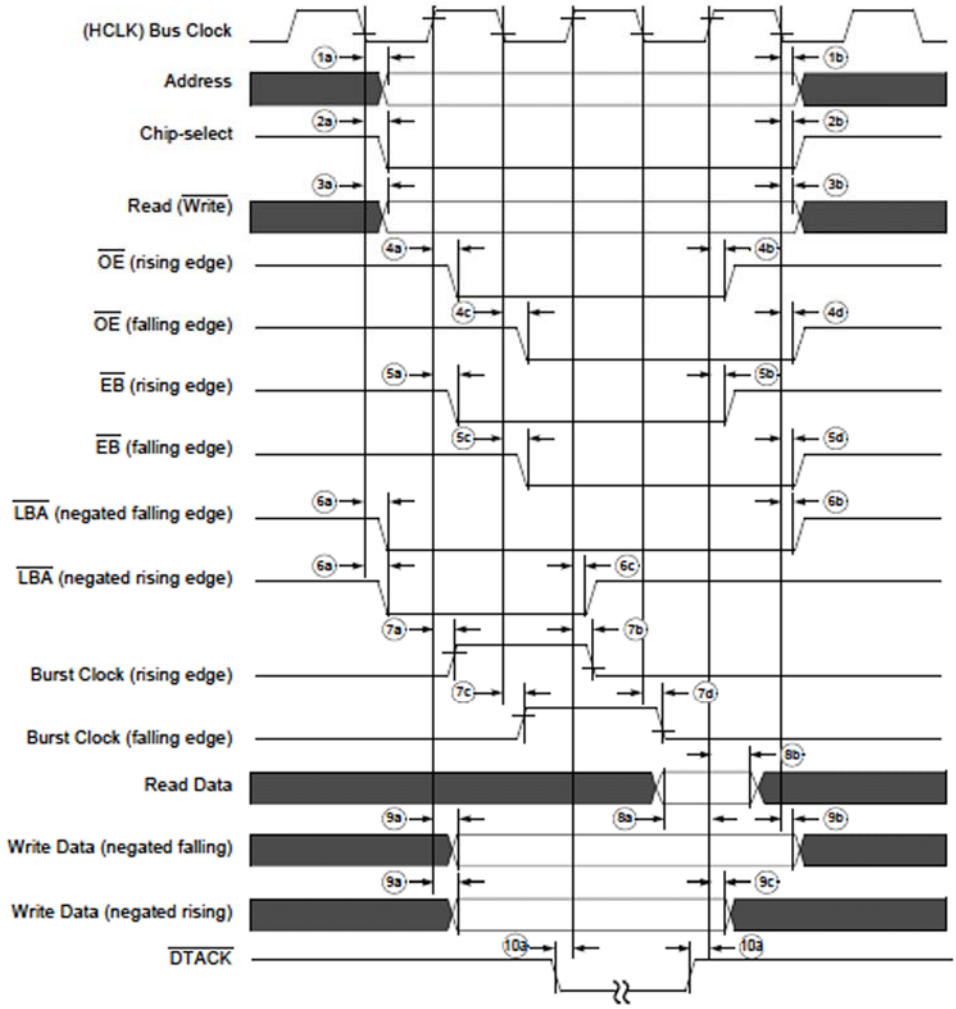


Figure 10.11: EIM Bus Timing Diagram

Revision history for Chapter 10

Edition	Date	Revised section	Content of revisions
0			First edition
1	05/04/11	Chapter 2.2	Modified maximum battery voltage (from 4.3 V to 5.0 V) due to changes in electrical specifications
2	05/06/17	Chapter 2.2	Added μT-Engine descriptions and changed battery voltage to 5.25 V, taking into consideration +/- 5% variation
3	05/09/29		Adjusted chapter and figure numbers due to merging documents

■ Chapter 11 TX4956 T-Engine expansion board design guidelines

This chapter describes design guidelines for expansion boards connecting via the expansion slot on a T-Engine/TX4956 T-Engine.

The expansion board refers to a board featuring user selected devices etc. and controllable using the TX4956 address bus, data bus, and PCI bus output to the T-Engine expansion bus connector.

11.1. T-Engine expansion bus connector specifications

T-Engine connector type implemented: 20-5603-14-0404-861+ (Kyocera Elco)

Compatible connector type: 10-5603-14-0404-861+ (Kyocera Elco)

Figure 11.1 shows the arrangement of the expansion bus connector.

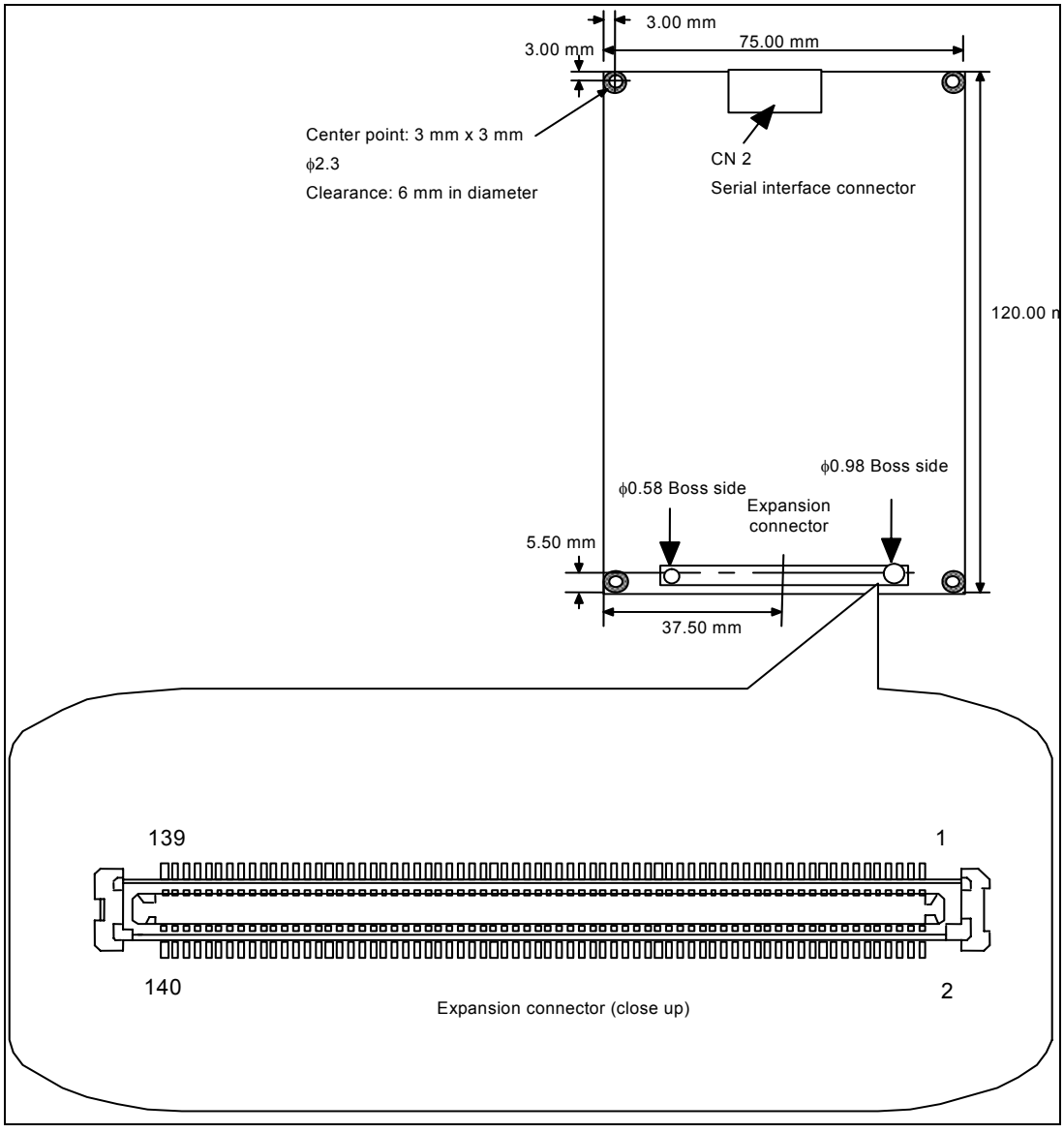


Figure 11.1: Expansion bus connector arrangement

11.2. Expansion bus connector signal arrangement

Table 11.2 shows the arrangement of expansion slot signals.

Both PCI bus and local bus signals are used. The electrical power level is 3.3 V.

Table 11.2: Expansion slot signal arrangement

Pin No.	Signal	I/O	Pin No.	Signal	I/O	Pin No.	Signal	I/O	Pin No.	Signal	I/O
1	GND	-	36	PAD20	I/O	71	PAD2	I/O	106	LA1	OUT
2	PCICLK2	OUT	37	GND	-	72	PAD3	I/O	107	LA8	OUT
3	GND	-	38	PAD18	I/O	73	GND	-	108	LA0	OUT
4	PCICLK1	OUT	39	GND	-	74	PAD1	I/O	109	LWE1#	OUT
5	GND	-	40	PAD17	I/O	75	GND	-	110	LWE0#	OUT
6	PCICLK0	OUT	41	PCI_CBE3#	I/O	76	PAD0	I/O	111	GND	-
7	PCI_REQ2#	IN	42	PAD16	I/O	77	PCI_RESET#	OUT	112	LRD#	OUT
8	3.3V *1	OUT	43	PCI_CBE2#	I/O	78	LOBAT#	IN(O/D)	113	LD15	I/O
9	PCI_REQ1#	IN	44	PCI_STOP#	I/O	79	SHDN#	OUT	114	LD7	I/O
10	3.3V *1	OUT	45	PCI_LOCK#	I/O	80	PCI_INTA#	IN(O/D)	115	LD14	I/O
11	PCI_REQ0#	IN	46	PCI_PERR#	I/O	81	WAKEUP#	IN(O/D)	116	LD6	I/O
12	PCI_GNT2#	OUT	47	PCI_IRDY#	I/O	82	PCI_INTB#	IN(O/D)	117	LD13	I/O
13	GND	-	48	PCI_TRDY#	I/O	83	Reserved	-	118	LD5	I/O
14	PCI_GNT1#	OUT	49	GND	-	84	PCI_INTC#	IN(O/D)	119	LD12	I/O
15	GND	-	50	PCI_FRAME#	I/O	85	Reserved	-	120	LD4	I/O
16	PCI_GNT0#	OUT	51	GND	-	86	Reserved	-	121	LD11	I/O
17	PAD31	I/O	52	PCI_DEVSEL#	I/O	87	LA17	OUT	122	LD3	I/O
18	IDSEL2(PAD29)	OUT	53	PCI_PAR	I/O	88	FCS1#	OUT	123	LD10	I/O
19	PAD30	I/O	54	PCI_SERR#	IN(O/D)	89	LA16	OUT	124	LD2	I/O
20	IDSEL1(PAD28)	OUT	55	PCI_CBE1#	I/O	90	FCS0#	OUT	125	LD9	I/O
21	PAD29	I/O	56	PAD15	I/O	91	LA15	OUT	126	LD1	I/O
22	IDSEL0(PAD27)	OUT	57	PCI_CBE0#	I/O	92	IORDY#	IN(O/D)	127	LD8	I/O
23	PAD27	I/O	58	PAD14	I/O	93	GND	-	128	LD0	I/O
24	PAD28	I/O	59	PAD12	I/O	94	LA7	OUT	129	VBATT_IN *2	IN
25	GND	-	60	PAD13	I/O	95	LA14	OUT	130	VBATT_IN *2	IN
26	PAD26	I/O	61	GND	-	96	LA6	OUT	131	VBATT_IN *2	IN
27	GND	-	62	PAD11	I/O	97	LA13	OUT	132	VBATT_IN *2	IN
28	PAD25	I/O	63	GND	-	98	LA5	OUT	133	VBATT_IN *2	IN
29	PAD23	I/O	64	PAD10	I/O	99	LA12	OUT	134	VBATT_IN *2	IN
30	PAD24	I/O	65	PAD8	I/O	100	LA4	OUT	135	VBATT_IN *2	IN
31	PAD22	I/O	66	PAD9	I/O	101	LA11	OUT	136	VBATT_IN *2	IN
32	Reserved	-	67	PAD6	I/O	102	LA3	OUT	137	GND	-
33	PAD21	I/O	68	PAD7	I/O	103	LA10	OUT	138	GND	-
34	Reserved	-	69	PAD4	I/O	104	LA2	OUT	139	GND	-
35	PAD19	I/O	70	PAD5	I/O	105	LA9	OUT	140	GND	-

*1: When the CPU board's power is on, a power supply of +3.3 V (typ.) is provided to the expansion board.

*2: This terminal is used for the power supply (5.0 - 7.0 V) from the expansion board. Power can be supplied from the expansion board to the CPU board.

11.3. Areas over which the expansion board can be expanded

Table 11.3 shows the T-Engine/TX4956 memory map.

As shown in Table 11.3, the expansion board can be expanded to three areas: the PCI space, LDCS1, and LDCS2. Since the wait number and bus width for each area can be set by configuring the bus controller inside the VRC5477 on the T-Engine/TX4956, devices with different access speeds and different bus widths can be used together.

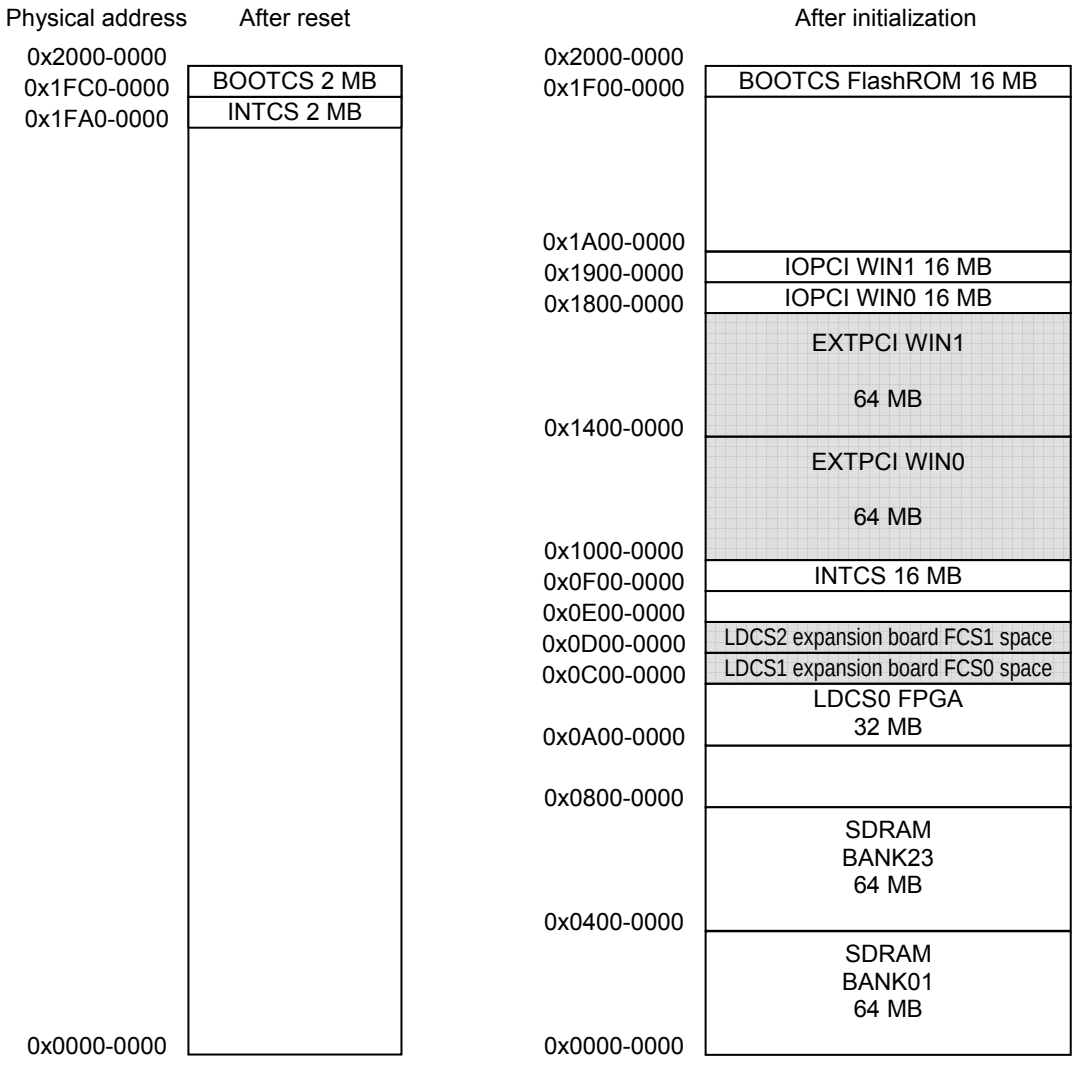


Table 11.3: VR5500 memory map

11.4. Power supply to the expansion board

Table 11.4 shows the voltage and current of the power supply available from the T-Engine to the expansion board. If the expansion board needs power in excess of this supply, additional steps must be taken to provide a power supply on the expansion board.

The power supply figures shown in Table 11.4 are for reference purposes only and are not guaranteed.

Table 11.4: Voltage and current of the power supply available to an expansion board

Expansion bus connector signal	Voltage output	Allowable current	Notes
3.3 V	+3.3 V	800 mA	Supplied when the board's power is on

11.5. Interrupt inputs from the expansion board

T-Engine features three interrupt input terminals on the expansion bus connector for use in input of interrupts from the expansion board: PCI_INTA#, PCI_INTB#, and PCI_INTC#. Figure 11.5 shows the interrupt terminal structure on the T-Engine expansion bus connector.

Each interrupt terminal in the expansion bus connector recognizes low level interrupts. After the VRC5477 recognizes an interrupt, it issues an interrupt to the TX4956. Settings for interrupts sent from the VRC5477 to the TX4956 are configured in the VRC5477's register.

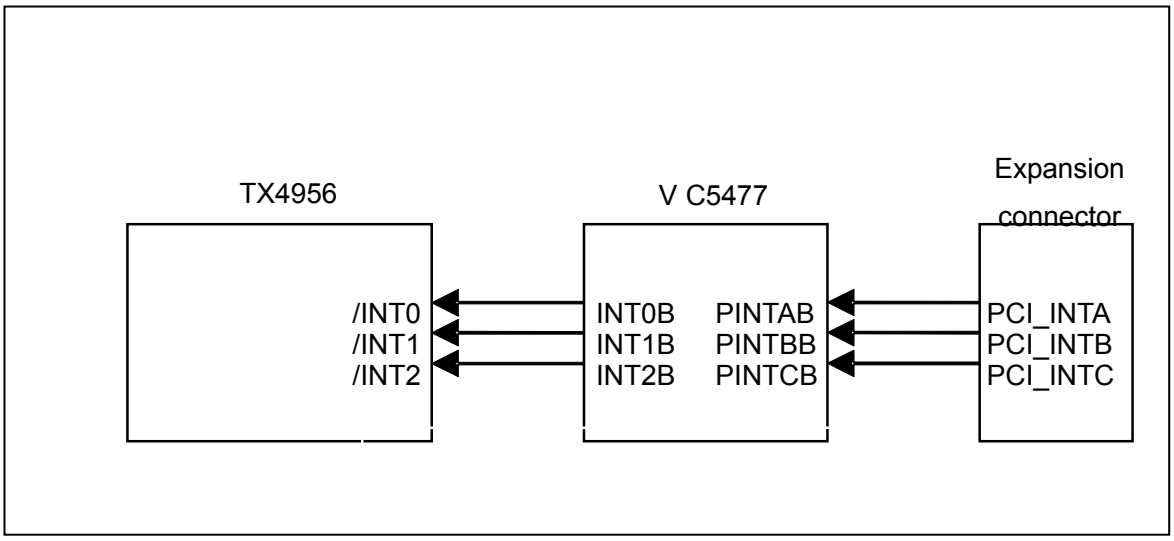


Figure 11.5: Interrupt terminal structure on T-Engine expansion bus connector

11.6. Expansion board stacking numbers

Use care with regard to power capacity when stacking multiple expansion boards.

Figure 11.6 shows an expansion board stacking structure.

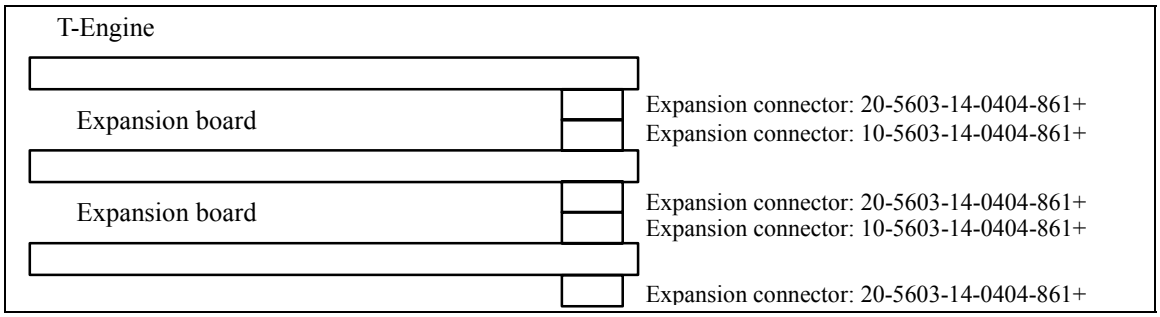


Figure 11.6: Expansion board stacking structure

11.7. /WAIT inputs

µT-Engine has one IORDY# input terminal on its expansion bus connector, for expansion board /WAIT input. When outputting a WAIT signal from the expansion board, be sure to use open collector output to prevent collision between /WAIT outputs when stacking multiple expansion boards. The IORDY# terminal on the µT-Engine side is pulled up at 4.7 kΩ. Figure 11.7 shows a structural diagram for the IORDY# terminal in an expansion bus connector.

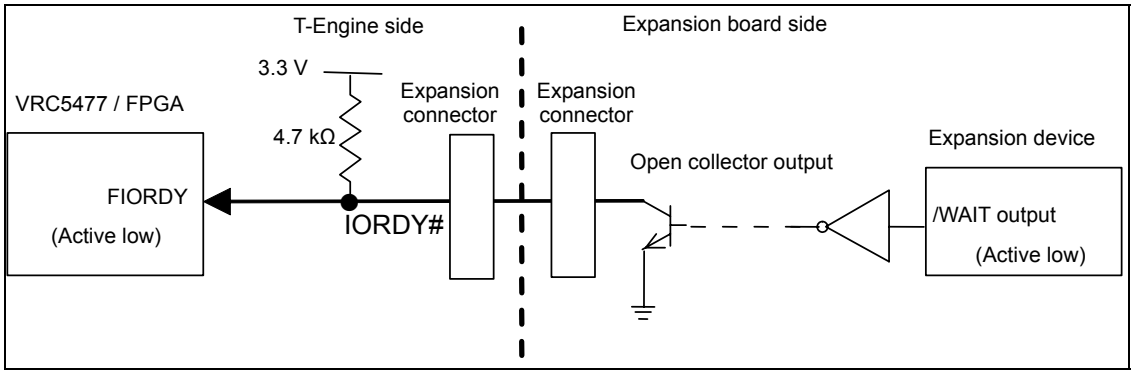


Figure 11.7: Structural diagram for IORDY# terminal in expansion bus connector

11.8. AC timing

As shown in Figure 11.8, the local bus signals output to the expansion bus connector are output via the bus buffer. For this reason, the bus signal is delayed vs. the timing of the VRC5477 bus. Be sure to take this delay into account when designing an expansion board. Bus timing is shown beginning on the following page.

For details of VRC5477 bus timing, refer to the VRC5477 hardware manual.

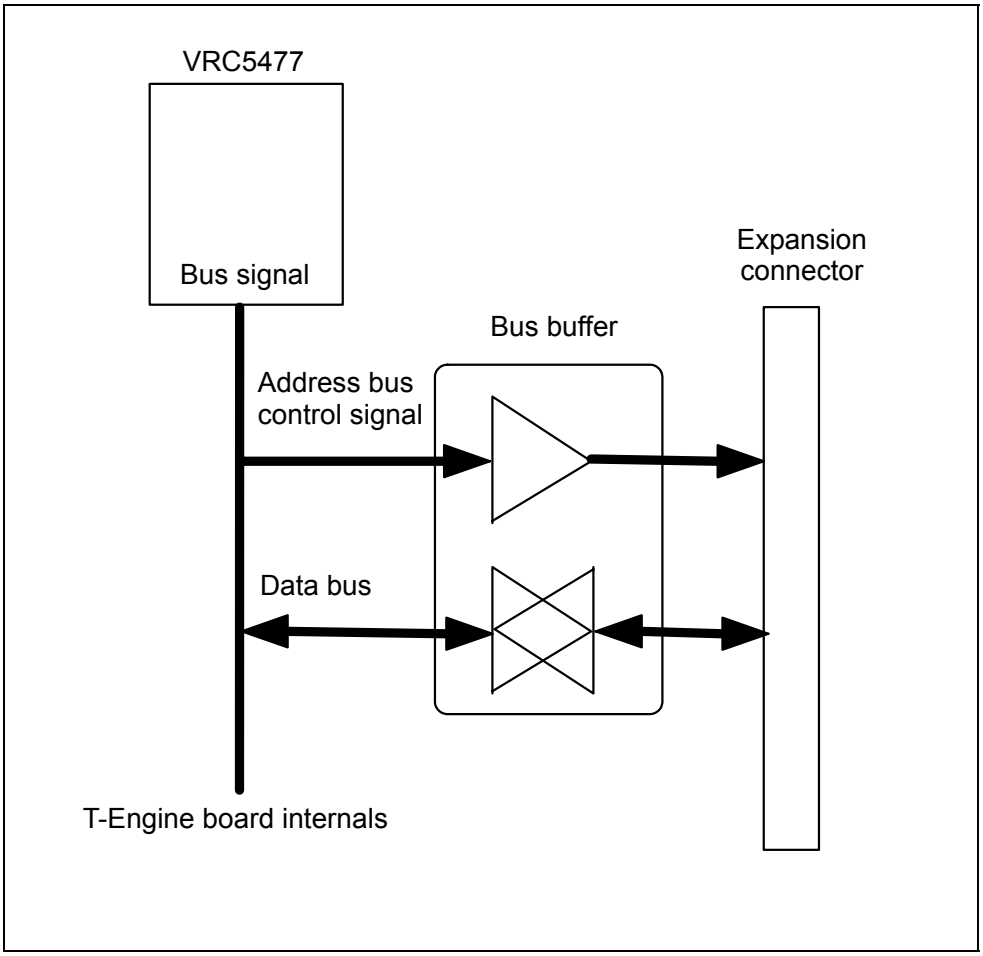
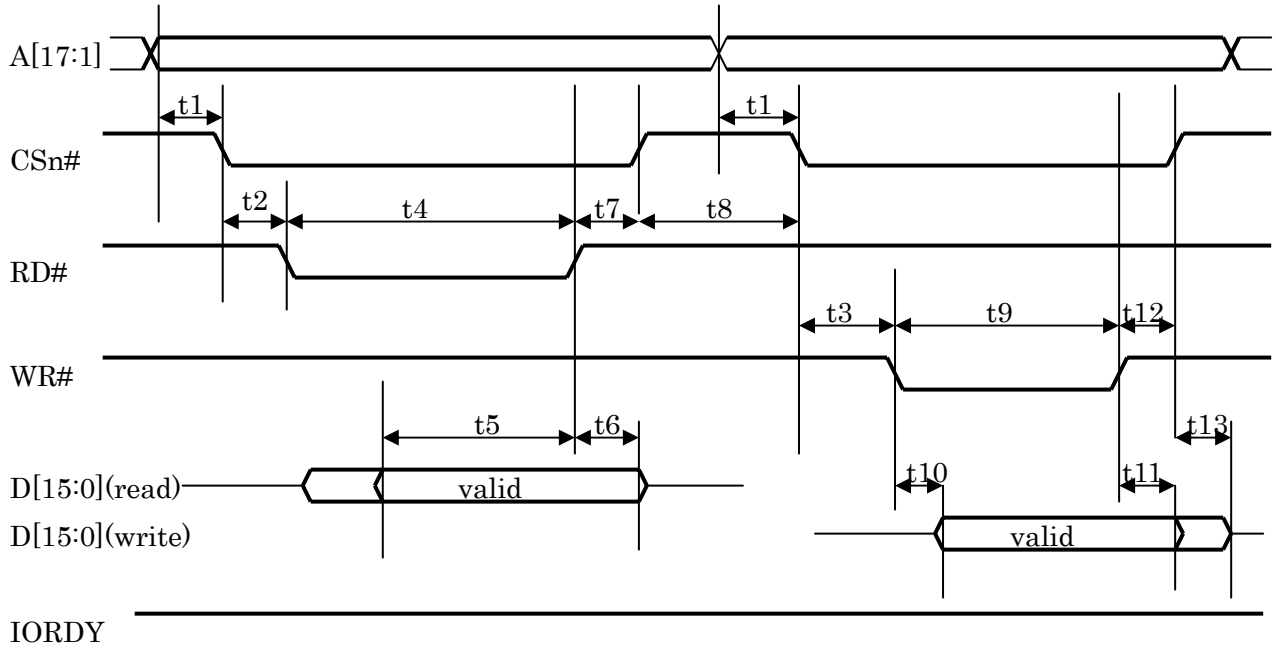


Figure 11.8: Expansion bus connector bus buffer structure

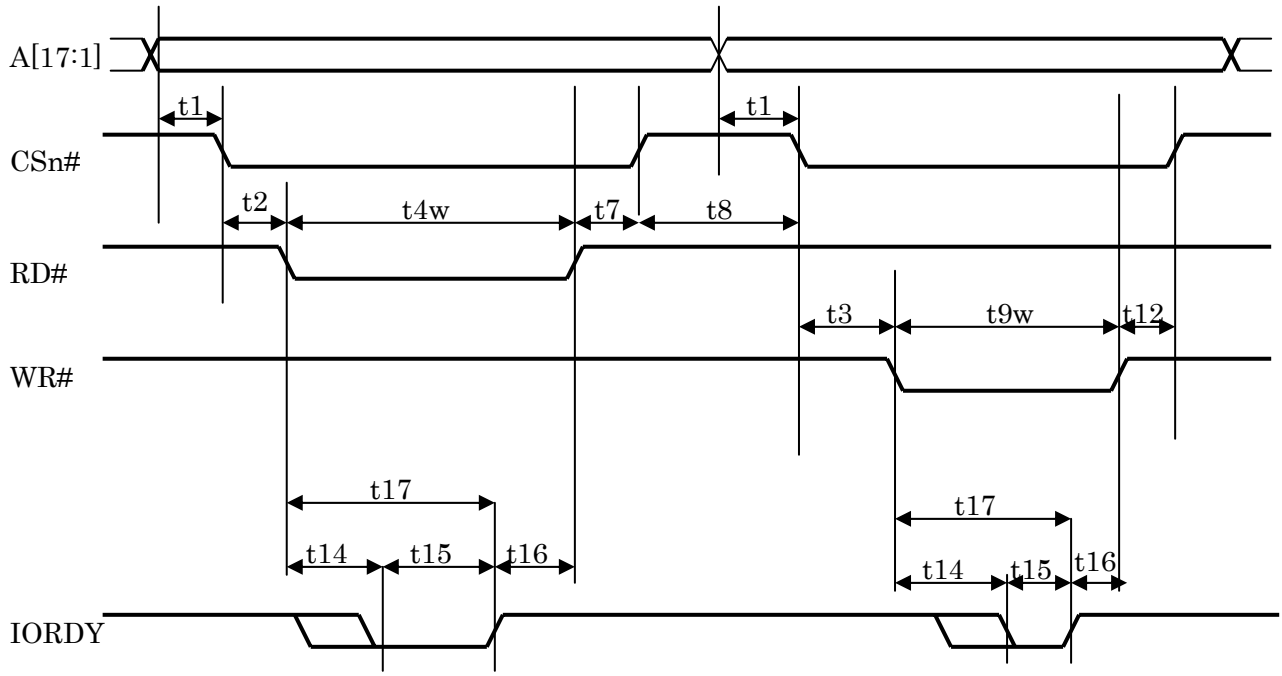
Note:

(1) The bus timing delay figure given above is for reference purposes only and is not guaranteed.

• Expansion bus READ/WRITE timing



• Expansion bus IORDY timing



• Expansion bus specifications

Symbol	Description	Min [nS]	Max [nS]
t1	Address valid to CSn# ↓ delay	0	
t2	CSn # ↓ toRD# ↓ delay	0	
t3	CSn # ↓ to WR# ↓ delay	30	
t4	RD# pulse width	160	
t4w	RD# pulse width (with IORDY controlled)	190	
t5	Read data setup	40	
t6	Read data hold	0	30
t7	RD# ↑ to CSn# ↑ delay	0	
t8	CSn# idle width	25	
t9	WR# pulse width	160	
t9w	WR# pulse width (with IORDY controlled)	190	
t10	WR# ↓ to write data valid delay		45
t11	WR# ↑ to write data hold	20	
t12	WR# ↑ to CSn# ↑ delay	25	65
t13	CSn# ↑ to write data disable		25
t14	RD#/WR# ↓ to IORDY ↓ delay	0	120
t15	IORDY pulse width	70	
t16	IORDY ↑ to RD#/WR# ↑ delay	10	
t17	RD#/WR# ↓ to IORDY ↑ delay	190	

■ Chapter 12 Nios II μT-Engine expansion board design guidelines

This chapter describes design guidelines for Expansion boards connecting via the expansion slot on a μT-Engine/ Nios II (“μT-Engine” hereinafter).

The Expansion board refers to a board featuring user selected devices etc. and controllable using the Nios II general purpose I/O output to the μT-Engine expansion slot.

12.1. μT-Engine expansion slot specifications

Connector number: CN6

μT-Engine connector type implemented: 20-5603-14-0606-861+ (Kyocera Elco)

Compatible connector type: 10-5603-14-0606-861+ (Kyocera Elco)

Figure 12.1 shows the arrangement of the expansion slot.

Figure 12.2 shows the direction in which to install the expansion slot.

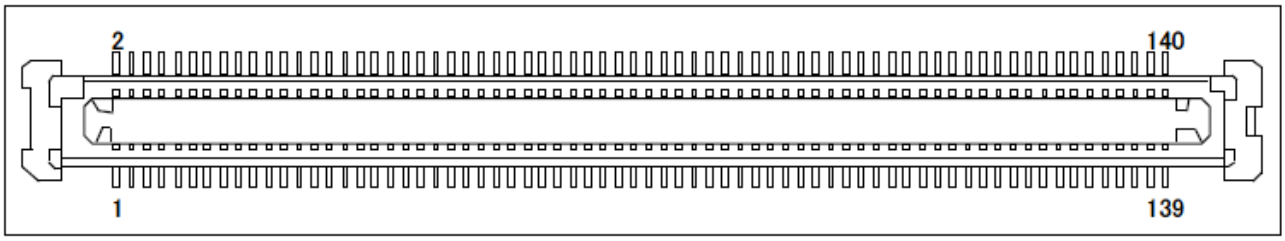


Figure 12.1: Arrangement of expansion slot

μT-Engine CPU board (underside)

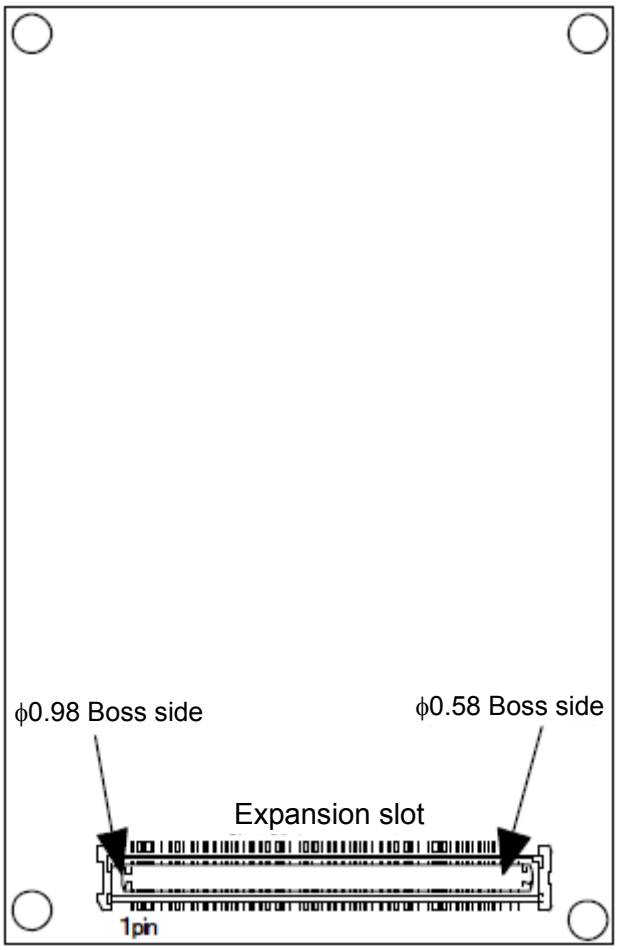


Figure 12.2: Direction in which to install expansion slot

12.2. Expansion slot signal arrangement

Table 12.2.1 shows the arrangement of signals when connecting the universal board included standard with the development kit.

With the exception of some specialized signals, the μT-Engine expansion slot can be redefined as the FPGA's general purpose I/O terminal.

Table 12.2.2 shows an example in which a user designs an expansion board independently.

Table 12.2.1: Expansion connector signal arrangement (when connecting the universal board included standard)

Pin No.	Signal	I/O	Pin No.	Signal	I/O	Pin No.	Signal	I/O	Pin No.	Signal	I/O
1	3.3 V		36	protolO25		71	ETXD	I	106	TCK	I
2	3.3 V		37	rotolO26		72	ECTS#	I	107	TMS	I
3	3.3 V		38	rotolO27		73	EFIXD	O	108	POWI#	O
4	3.3 V		39	GND	—	74	POWO#	I	109	TDI	I
5	GND		40	GND	—	75	GND	—	110	TDO	O
6	GND		41	rotolO28		76	GND	—	111	GND	—
7	GND		42	rotolO29		77	MICTOR0		112	GND	—
8	GND		43	rotolO30		78	MICTOR1		113	EOSC	O
9	protolO0		44	rotolO31		79	MICTOF12		114	GND	—
10	protolO1		45	rotolO32		80	MICTOR3		115	ECLKIN	O
11	protolO2		46	rotolO33		81	MICTOR4		116	GND	—
12	protolO3		47	rotolO34		82	MICTOR5		117	ECLKOUT	I
13	protolO4		48	rotolO35		83	MICTOR6		118	GND	—
14	protolO5		49	rotolO36		84	MICTOR7		119	GND	—
15	protolO6		50	rotolO37		85	MICTOR8		120	GND	—
16	protolO7		51	rotolO38		86	MICTOR9		121	CONF_ DONE	O
17	protolO8		52	rotolO39		87	MICTOR10		122	—	—
18	protolO9		53	rotolO40		88	MICTOR11		123	3.3 V	—
19	protolO10		54	CARDSEL#	I	89	MICTOR12		124	3.3 V	—
20	protolO11		55	ULEDO	O	90	MICTOR13		125	3.3 V	—
21	GND	—	56	ULEDI	O	91	MICTOR14		126	3.3 V	—
22	GND	—	57	GND	—	92	MICTOR15		127	Vunreg	—
23	protolO12		58	GND	—	93	GND	—	128	Vunreg	—
24	protolO13		59	ULED2	0	94	GND	—	129	Vunreg	—
25	protolO14		60	ULED3	0	95	MICTOR16		130	Vunreg	—
26	protolO15		61	ULED4	0	96	MICTOR17		131	Vunreg	—
27	protolO16		62	ULED5	0	97	MICTOR18		132	Vunreg	—
28	protolO17		63	ULED6	0	98	MICTOR19		133	Vunreg	—
29	protolO18		64	ULED7	0	99	MICTOF120		134	Vunreg	—
30	protolO19		65	PB_RESET#	I	100	MICTOF121		135	Vunreg	—
31	protolO20		66	USER_PB#O	I	101	MICTOF122		136	Vunreg	—
32	protolO21		67	USER_PB#I	I	102	MICTOF123		137	GND	—
33	protolO22		68	USER_PB#2	I	103	MICTOF124		138	GND	—
34	protolO23		69	USER_PB#3	I	104	TR_CLK	O	139	GND	—
35	protolO24		70	ERTS#	0	105	MICTOR_CLK	O	140	GND	—

With the exception of those related to power supply, all signal wires have electrical levels of 3.3 V.

A universal board features the following functions from among the various I/O types included on Altera's Nios (II) Development Board Cyclone Edition. The signals for realization of these functions are defined.

1: protoIO[39:0] is used by the Expansion Prototype Connector

2: MICTOR[24:0], TR_CLK, MICTOR_CLK, TCK, TMS, TDI, and TDO are used for connecting to the JTAG debugger

3: ETXD, ERXD, ERTS#, and ECTS# are used for serial communication

4: ULED[7:0] is used by dot LED devices
USER_PB#[3:0] is used by button switches

Table 12.2.2: Expansion connector signal arrangement (when the user designs an expansion board independently)

Pin No.	Signal/ terminal no.	I/O	Pin No.	Signal/ terminal no.	I/O	Pin No.	Signal/ terminal no.	I/O	Pin No.	Signal/ terminal no.	I/O
1	3.3 V	-	36	U6	(*1)	71	Y12	(*1)	106	L19 (TCK)	I
2	3.3 V	-	37	T6	(*1)	72	W12	(*1)	107	L16 (TMS)	I
3	3.3 V	-	38	R6	(*1)	73	(*1)	108	108	(*1)	
4	3.3 V	-	39	GND	-	74	U12	(*1)	109	K18 (TDI)	I
5	GND	-	40	GND	-	75	GND	-	110	L20 (TDO)	○
6	GND	-	41	Y7	(*1)	76	GND	-	111	GND	-
7	GND	-	42	W7	(*1)	77	Y13	(*1)	112	GND	-
8	GND	-	43	V7	(*1)	78	W13	(*1)	113	50MHz	o
9	UI	(*1)	44	U7	(*1)	79	V13	(*1)	114	GND	-
10	RI	(*1)	45	T7	(*1)	80	U13	(*1)	115	L8 (PLLI_OUT)	○
11	V2	(*1)	46	R7	(*1)	81	T13	(*1)	116	GND	-
12	U2	(*1)	47	Y8	(*1)	82	Y14	(*1)	117	K6 (CLKI)	I
13	T2	(*1)	48	W8	(*1)	83	W14	(*1)	118	GND	-
14	R2	(*1)	49	V8	(*1)	84	V14	(*1)	119	GND	-
15	W3	(*1)	50	U8	(*1)	85	U14	(*1)	120	GND	-
16	V3	(*1)	51	T8	(*1)	86	T14	(*1)	121	L18	0
17	U3	(*1)	52	Y9	(*1)	87	Y15	(*1)	122	-	-
18	T3	(*1)	53	W9	(*1)	88	W15	(*1)	123	3.3V	-
19	R3	(*1)	54	V9	(*1)	89	V15	(*1)	124	3.3V	-
20	Y4	(*1)	55	U9	(*1)	90	U15	(*1)	125	3.3V	-
21	GND	-	56	T9	(*1)	91	T15	(*1)	126	3.3V	-
22	GND	-	57	GND	-	92	W16	(*1)	127	Vunreg	-
23	W4	(*1)	58	GND	-	93	GND	-	128	Vunreg	-
24	V4	(*1)	59	R9	(*1)	94	GND	-	129	Vunreg	-
25	U4	(*1)	60	Y10	(*1)	95	V16	(*1)	130	Vunreg	-
26	T4	(*1)	61	W10	(*1)	96	U16	(*1)	131	Vunreg	-
27	R4	(*1)	62	V10	(*1)	97	T16	(*1)	132	Vunreg	-
28	W5	(*1)	63	U10	(*1)	98	Y17	(*1)	133	Vunreg	-
29	V5	(*1)	64	T10	(*1)	99	W17	(*1)	134	Vunreg	-
30	U5	(*1)	65	Y11	(*1)	100	V17	(*1)	135	Vunreg	-
31	T5	(*1)	66	W11	(*1)	101	U17	(*1)	136	Vunreg	-
32	R5	(*1)	67	V11	(*1)	102	T17	(*1)	137	GND	-
33	Y6	(*1)	68	U11	(*1)	103	W18	(*1)	138	GND	-
34	W6	(*1)	69	T11	(*1)	104	U18	(*1)	139	GND	-
35	V6	(*1)	70	R11	(*1)	105	L8 (PLL1_OUTp)	0	140	GND	-

*1: This is the FPGA (EP1C20F400C7) terminal no.

Although the electrical level used is 3.3 V, this level is programmable for the LVTTL and LVCMOS. For details, see Altera's Cyclone Device Handbook.

12.3. Expansion board size

It is recommended that an expansion board have the same size (85 mm x 60 mm) as a μT-Engine CPU board.

12.4. Power supply to the Expansion board

Table 12.4 shows the voltage and current of the power supply available from the μT-Engine to the Expansion board. If the Expansion board needs power in excess of this supply, additional steps must be taken to provide a power supply on the Expansion board. The electric current figures shown in Table 12.4 are tentative.

Table 12.4: Voltage and current of the power supply available to a Expansion board

Expansion bus connector signal	Voltage output	Allowable current	Notes
3.3 V	3.3 V	500 mA	
Vunreg	6.0 V		Can be supplied only when the AC adapter is connected.

12.5. Expansion board stacking numbers

Up to two Expansion boards may be stacked.

Use care with regard to power capacity when stacking multiple Expansion boards.

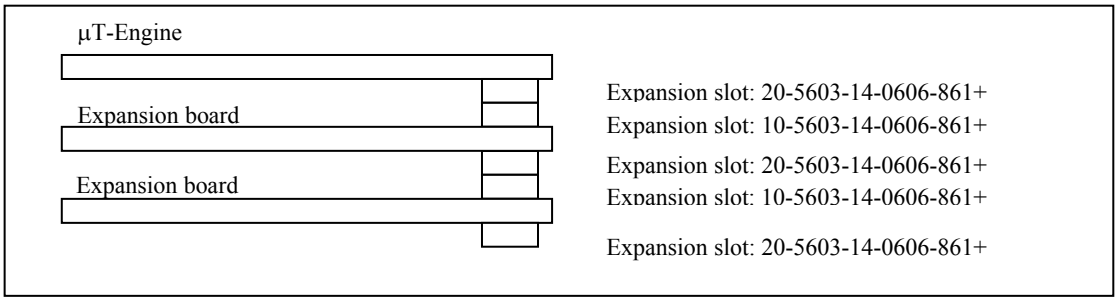


Figure 12.5: Expansion board stacking structure

■ Chapter 13 Ansel-Tea/FR T-Engine Appliance expansion board design guidelines

This chapter describes design guidelines for expansion boards connecting via the expansion slot on an Ansel-Tea/FR T-Engine Appliance.Expansion board as used here refers to a board featuring user selected devices etc. and controllable using the Ansel-Tea/FR T-Engine Appliance's address bus, data bus, and various control signals output to the T-Engine expansion bus connector.

13.1. T-Engine expansion bus connector specifications

T-Engine connector type implemented: 20-5603-14-0105-861+ (Kyocera Elco)
Compatible connector type: 10-5603-14-0105-861+ (Kyocera Elco)

Figure 13.1 shows the arrangement of the expansion bus connector.

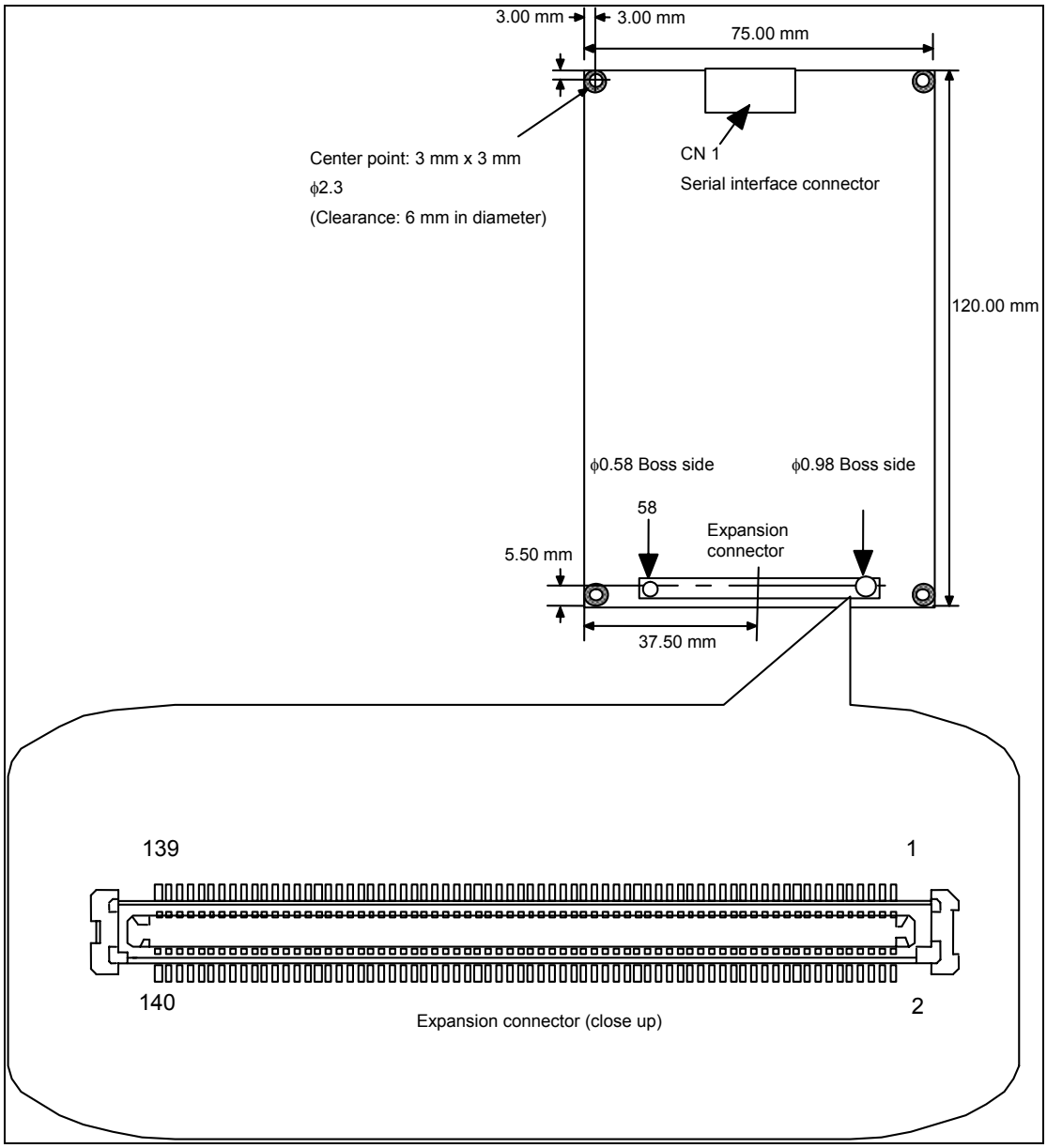


Figure 13.1: Expansion bus connector arrangement

13.2. Expansion bus connector signal arrangement

Table 13.2 shows the signal arrangement of an expansion bus connector.

This board features a 140-pin external expansion bus connector. The address bus, data bus, various control lines, and power supply are output to the connector, and various boards such as a battery board, a LAN board, an expansion FPGA board, and specialized user boards can be connected to it. The following table shows pin arrangements (manufacturer: Kyocera Elco; model no.: 2x 5603 14 0105 861).

No.	Signal	I/O
1	**EXB 5V**	-
2	**EXB 5V**	-
3	**EXB 5V**	-
4	**EXB 5V**	-
5	**EXB 5V**	-
6	**EXB 5V**	-
7	D0	I/O
8	D1	I/O
9	D2	I/O
10	D3	I/O
11	D4	I/O
12	D5	I/O
13	D6	I/O
14	D7	I/O
15	D8	I/O
16	D9	I/O
17	D10	I/O
18	D11	I/O
19	D12	I/O
20	D13	I/O
21	D14	I/O
22	D15	I/O
23	**GND**	
24	**GND**	
25	D16	I/O
26	D17	I/O
27	D18	I/O
28	D19	I/O
29	D20	I/O
30	D21	I/O
31	D22	I/O
32	D23	I/O
33	D24	I/O
34	D25	I/O
35	D26	I/O

No.	Signal	I/O
36	D27	I/O
37	D28	I/O
38	D29	I/O
39	D30	I/O
40	D31	I/O
41	**GND**	
42	**GND**	
43	A0	OUT
44	AI	OUT
45	A2	OUT
46	A3	OUT
47	A4	OUT
48	A5	OUT
49	A6	OUT
50	A7	OUT
51	A8	OUT
52	A9	OUT
53	A10	OUT
54	A11	OUT
55	A12	OUT
56	A13	OUT
57	A14	OUT
58	A15	OUT
59	**GND**	
60	**GND**	
61	A16	OUT
62	A17	OUT
63	A18	OUT
64	A19	OUT
65	A20	OUT
66	A21	OUT
67	A22	OUT
68	A23	OUT
69	CS0#	OUT
70	CS1#	OUT

No.	Signal	I/O
71	CS2#	OUT
72	CS3#	OUT
73	WEI #	OUT
74	R/W	OUT
75	**GND**	-
76	**GND**	-
77	CLK	OUT
78	BE2#	OUT
79	**GND**	-
80	BE3#	OUT
81	0E#	OUT
82	RESERVED	
83	BREQ #	I
84	BACK#	O
85	BE0#	O
86	BE1#	O
87	WAIT#	I
88	DE0T#	O
89	DREQ0#	I
90	DREQ1#	I
91	DACK2#	O
92	DACK1#	O
93	**GND**	-
94	**GND**	-
95	N.C.	
96	FPTOUT0	O
97	N.C.	
98	FPTOUT1	O
99	N.C.	
100	FPTOUT2	O
101	N.C.	
102	N.C.	
103	N.C.	
104	N.C.	
105	N.C.	

No.	Signal	I/O
106	N.C.	
107	**GND**	-
108	**GND**	-
109	N.C.	
110	N.C.	
111	FWEX	O
112	N.C.	
113	N.C.	
114	N.C.	
115	N.C.	
116	VTref	
117	N.C.	
118	BATTERY	I/O
119	N.C.	
120	advise EME	I
121	**GND**	-
122	**GND**	-
123	INT	I
124	nRESETO	O
125	PORST#	O
126	RTCK	O
127	RESET#	O
128	TRST#	I
129	TCK	I
130	TMS	I
131	TDI	I
132	TD0	O
133	**VBAT**	-
134	**VBAT**	-
135	**VBAT**	-
136	**VBAT**	-
137	**GND**	-
138	**GND**	-
139	**GND**	-
140	**GND**	-

Table 13.2: Expansion connector signal arrangement

*1: When using a DipSW or the allocated I/O port, power of 5.0 V (typ.) is supplied.

*2: For use with inputs from the battery board. The main unit operates when 3.6 - 5.25 V is input.

13.3. Areas over which the expansion board can be expanded

Table 13.3 shows the memory map for the MB91403 on the Ansel-Tea/FR.

As shown in Table 13.3, the expansion board can be expanded to the CS6X area.

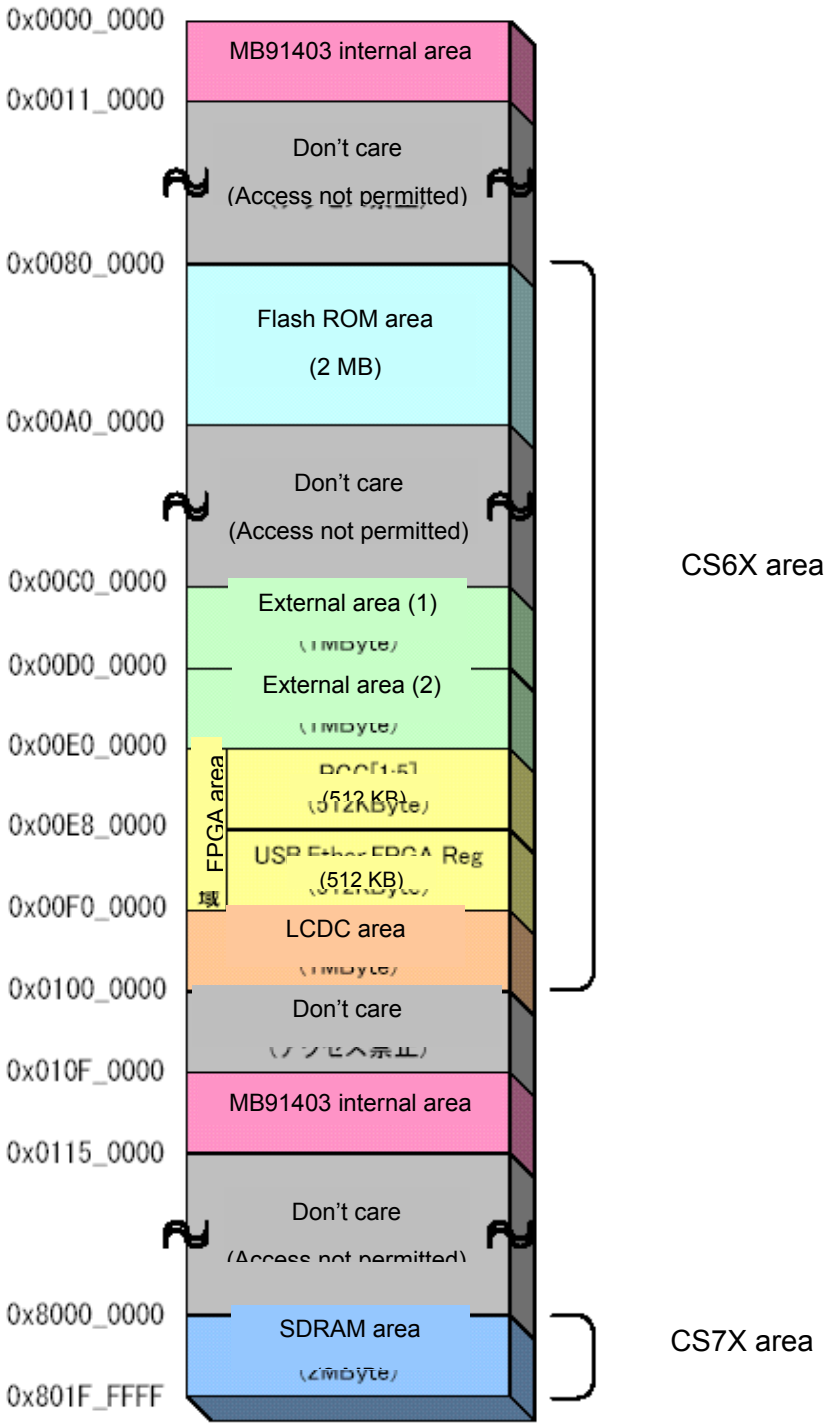


Table 13.3: MB91403 memory map

13.4. Power supply to the expansion board

Table 13.4 shows the voltage and current of the power supply available from the T-Engine to the expansion board. If the expansion board needs power in excess of this supply, additional steps must be taken to provide a power supply on the expansion board. These calculations are based on main unit power consumption of no more than 2 W and AC adapter output of 5.0 V and 2.0 A. The power supply figures shown in Table 13.4 are for reference purposes only and are not guaranteed.

Table 13.4: Voltage and current of the power supply available to an expansion board

Expansion bus connector signal	Voltage output	Allowable current	Notes
EXB 5 V	5.0 V	1400 mA(*1)	When using an AC adapter
EXB 5 V	5.0 V	370 mA(*1)(*2)	When using a battery board

*1: When running the USB host controller using bus power and when using a 5V PC card, deduct the power used.

*2: Calculations are based on a 0.5 A power supply from the battery board (TTZ101-003). This depends on the power consumption balance with the main board. When connecting a power supply other than a battery board to the VBAT terminal, this figure will vary depending on the capacity of the power supply connected.

13.5. Interrupt inputs from the expansion board

Figure 13.5 shows the interrupt connection structure for the Ansel-Tea/FR core board and base board and for an expansion board connected to the base board.

The MB91403 has two interrupt input terminals. One of these is assigned to interrupts (INT7) input from the FPGA on the base board and the other to interrupts (INT6) from the expansion board.

For details of interrupt controls, see the MB91403 interrupt specifications.

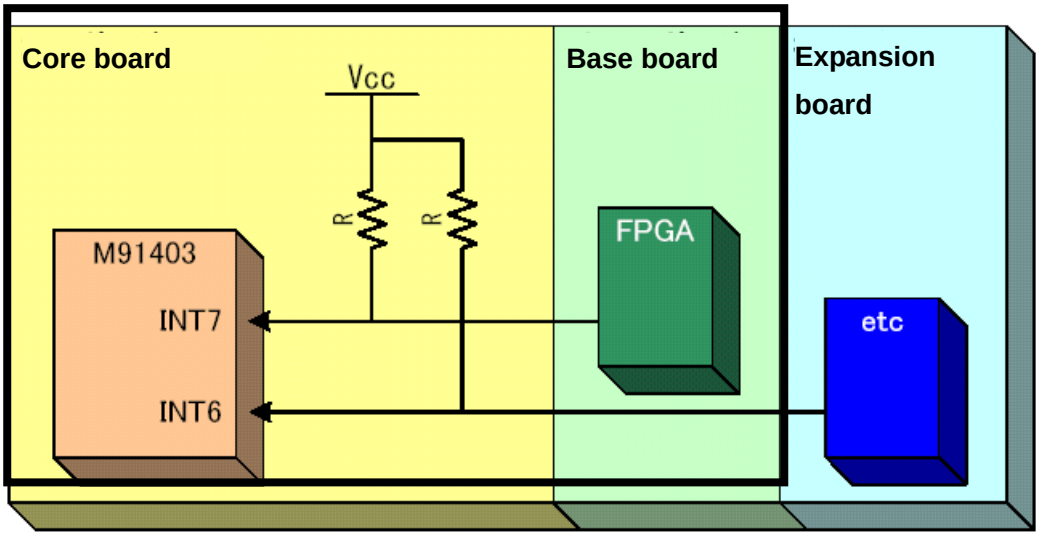


Figure 13.5: Ansel-Tea/FR interrupt signal connection structure

13.6. Expansion board stacking numbers

Use care with regard to power capacity when stacking multiple expansion boards.

Figure 13.6 shows an expansion board stacking structure.

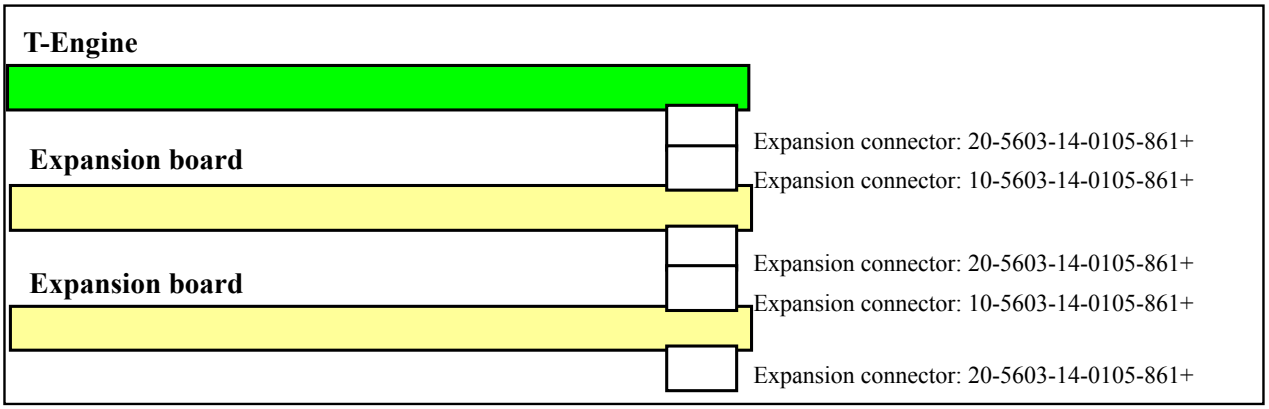


Figure 13.6: Expansion board stacking structure

13.7. /WAIT inputs

T-Engine has one /WAIT input terminal on its expansion bus connector, for expansion board /WAIT input. When outputting a WAIT signal from the expansion board, be sure to use open collector output to prevent collision between /WAIT outputs when stacking multiple expansion boards. The /WAIT terminal on the T-Engine side is pulled up at 680 Ω. Figure 13.7 shows a structural diagram for the /WAIT terminal in an expansion bus connector.

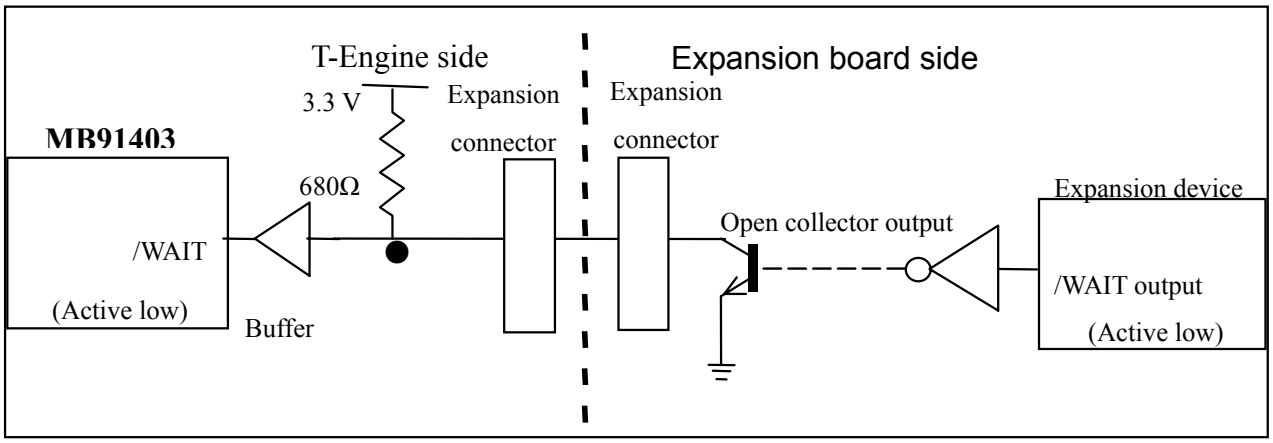


Figure 13.7: Structural diagram for /WAIT terminal in expansion bus connector

13.8. AC timing

Figure 13.8.1 shows an overview of the MB91403 bus signals output to the expansion bus connector. On this board, the connection to the expansion bus connector is made directly, without using a bus buffer.

Figure 13.8.2 shows the basic bus timing of the MB91403.

For details of MB91403 bus timing, refer to the MB91403 manual.

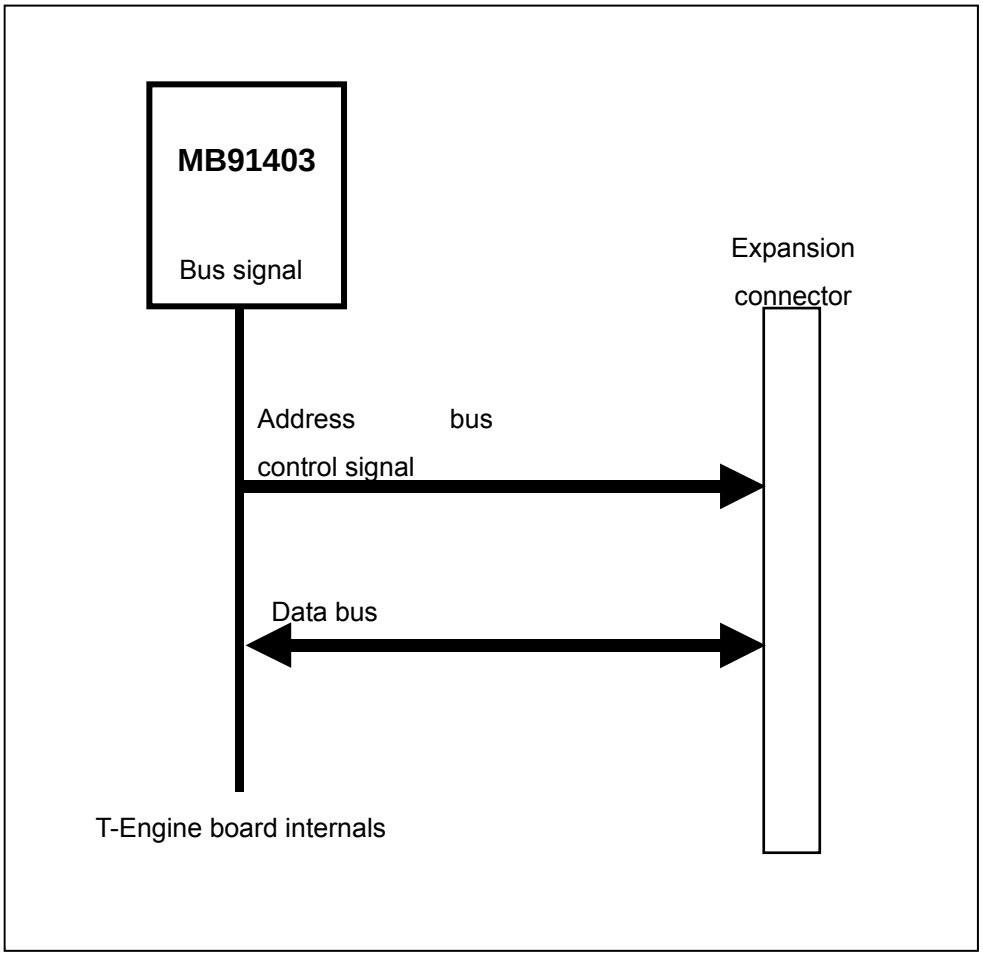


Figure 13.8: Expansion bus connector bus buffer structure

AC timing

(1) Ordinary memory access

Item	Signal	Terminal	Base timing	Standard values		Units	Notes
				Minimum	Maximum		
Address delay	tchav	MEMA[23:0]	MCLKO ↑	—	tcycp/2+7	ns	
CSX delay	tchcsi	MEMCSX[2:0]	MCLKO ↑	—	tcycp/2+7	ns	
CSX delay	tchcsh	MEMCSX[2:0]	MCLKO ↑	—	tcycp/2+7	ns	
WRX delay	tchwri	MEMWRX[3:0]	MCLKO ↑	—	9	ns	
WRX delay	tchwrh	MEMWRX[3:0]	MCLKO ↑	—	9	ns	
Data delay	tchdv	MEMD[31:0]	MCLKO ↑	—	tcycp/2+7	ns	
RDX delay	tchrdl	MEMRDX	MCLKO ↑	—	9	ns	
RDX delay	tchrdh	MEMRDX	MCLKO ↑	—	9	ns	
Data setup	tdsrh	MEMD[31:0]	MCLKO ↑	19	—	ns	
Data hold	trhdx	MEMD[31:0]	MCLKO ↑	-1	—	ns	

* tcycp: external memory clock cycle

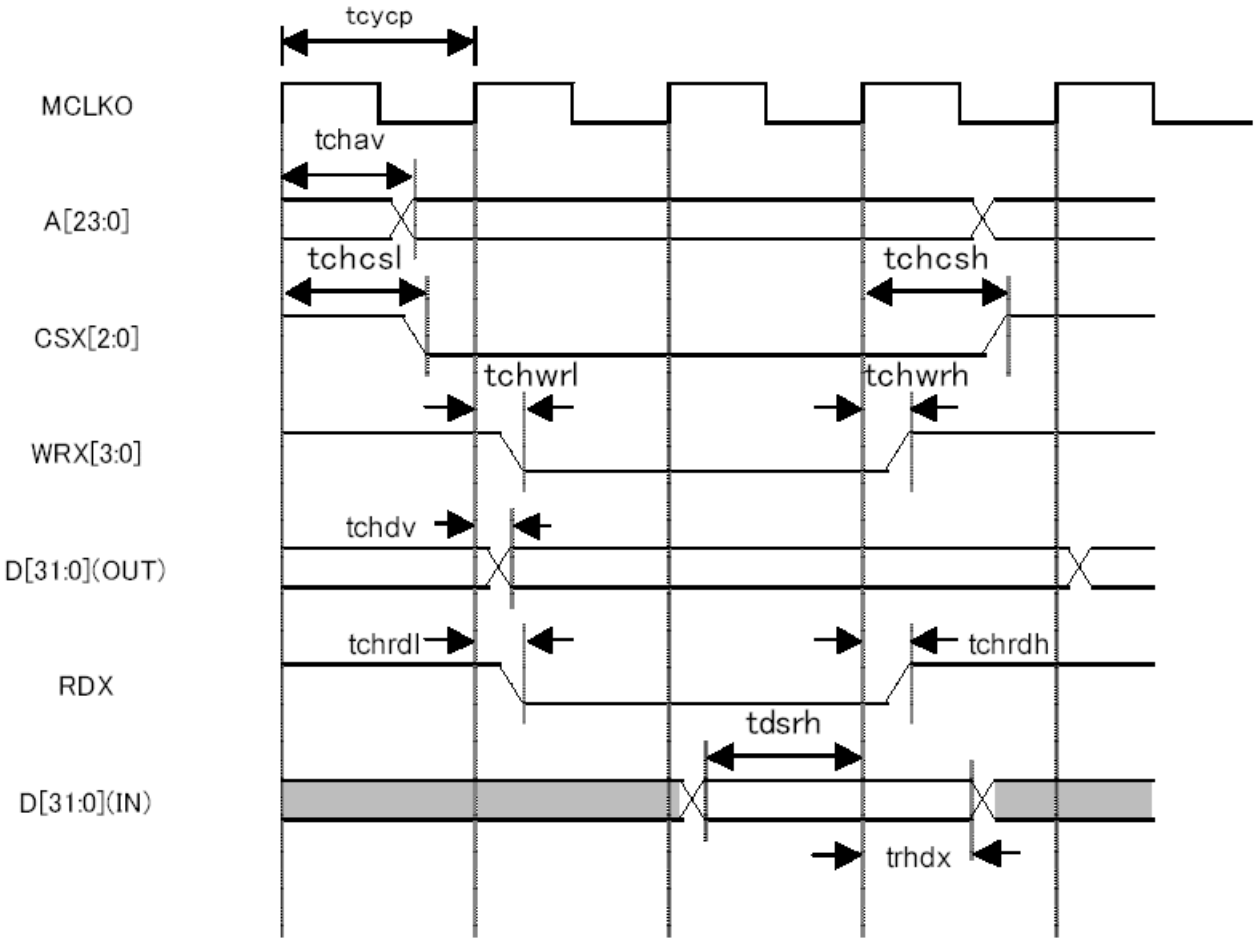


Figure 13.8.2: MB91403 basic bus timing

T-Engine Expansion Board Design Guideline (Ver.1.00.01)

TEF010-S008-01.00.01/en

June 2009

About this specification, please refer to follows;

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