T-Engine Design Guidelines

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T-Engine Forum

http://www.t-engine.org/

CONTENTS

Chapter 1 Overview of T-Engine specifications

1.1. Significance of the T-Engine project and standardization of hardware specifications

(1) Objective and positioning of the T-Engine project

The T-Engine project is a project intended to increase the efficiency of development of software for controlling embedded systems, by increasing the ease of distributing and reusing software components such as middleware and device drivers. Centered on the T-Kernel real-time operating system, T-Engine's appeal is in the way it makes it possible to standardize the specifications of device drivers and middleware, to improve the compatibility of software, and to develop high-quality software quickly and at low cost.

Effective means of improving software compatibility and development efficiency include not just standardization of specifications for software such as operating systems but also standardization of hardware specifications and development environments as well. In the precursor to the T-Engine project, the ITRON project, only the specifications of the real-time OS were standardized, with no particular standards established for hardware or development environments. As a result, there were cases in which software could not be ported smoothly even between ITRON devices and in which software components such as middleware and device drivers did not have sufficient ease of distribution or reuse. A major strong point of the T-Engine project is the substantial improvements it has made in this area by standardizing hardware and development environments as well. Specific details of this standardization are covered later.

Since the hardware used in embedded systems varies widely, standardization of the hardware specifications for embedded systems themselves (i.e., for the final products) is not possible. This is why the T-Engine project seeks to improve software development efficiency by standardizing the hardware specifications not of the hardware of final embedded system products but of development evaluation boards used for developing prototypes and for software distribution.

A development evaluation board is a board computer used for proceeding with software development and evaluation until the hardware of the final embedded system product (e.g., in the case of a mobile phone the same hardware that will be used in the final product, in the form of a compact mobile phone) is complete. There are two types of standard specifications available for hardware for this purpose: standard T-Engine board specifications and μT-Engine board specifications. Each can be used for its own suitable purposes.

Development using a standard T-Engine board or a μT-Engine board — each of which is a development evaluation board — is conducted in the following steps: first, software is developed to run on the standard T-Engine board or μT-Engine board, and then it is ported to the final hardware when that hardware is complete. Since these two steps are involved, it might seem that this development process is complex and troublesome. However, use of a standard T-Engine board or a μT-Engine board has the following benefits.

First of all, use of a standard T-Engine board or a μT-Engine board makes it possible to proceed with development of software for a final product even before the final hardware is complete. Also, building software to some extent on a standard T-Engine board or a μT-Engine board makes it possible to develop prototypes of the final products early. Such prototypes can be used for demonstration purposes and for evaluation and feedback,

resulting in product improvements. Since standard T-Engine boards and µT-Engine boards are commercially available, if they are in stock developers can purchase and use them immediately, making it possible to proceed with software development using a structure close to that of the final product even if details of the hardware specifications for the final product have not yet been decided on or hardware development is delayed.
(See Figure 1.1.1)

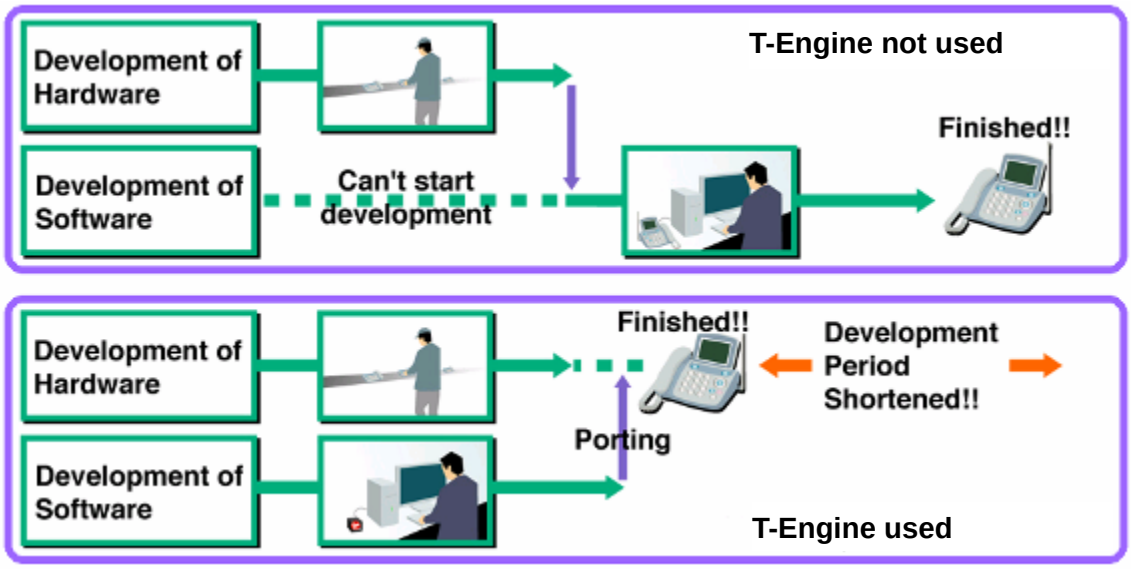


Figure 1.1.1: Using T-Engine to shorten the development period for an embedded system

Another benefit is the fact that standardization of the hardware specifications of the standard T-Engine and µT-Engine boards makes it possible to distribute software components such as OSs, middleware, and device drivers that run on such hardware as object code. As explained at the start of this chapter, the chief objective of the T-Engine project is improving the ease of distribution and reuse of software components such as middleware and device drivers. Enabling distribution of OSs and software components as object code in the same way as retail PC software or games is a major benefit toward achieving this goal.

In the past, when a developer wanted to test and evaluate software for embedded systems in an environment similar to that of a product under development, he or she needed to obtain the relevant source program and adjust and port it to make it executable on the hardware under development. However, not only does obtaining the source program in such a case often require payment of high costs, but another problem it involved was the difficulty in use for evaluation purpose due to the requirement of complex steps such as porting and compiling. In the T-Engine project, in addition to standardization of the T-Kernel real-time OS and a device driver API, standardization of the standard T-Engine and µT-Engine development evaluation boards resolves this problem by making it possible to distribute software components as object code.

On the other hand, the hardware specifications of the final embedded system product (e.g., the hardware specifications of a mobile phone developed using T-Engine) need not adhere to standard T-Engine or µT-Engine hardware specifications. These can be decided on freely in accordance with individual product plans and required specifications. For example, although the standard T-Engine board has a USB terminal, if USB is not needed for the final product it may be left out. Also, while board sizes and expansion bus connectors are standardized for the

standard T-Engine and μT-Engine development evaluation boards, final hardware need not be bound by these specifications. Although this point does not directly involve persons developing products using the standard T-Engine and μT-Engine boards, it is often misunderstood when developing T-Engine-based products, and as such should be noted.

Development evaluation boards used solely in connection with developing software for embedded systems using T-Kernel need not necessarily comply strictly with the standard T-Engine and μT-Engine board hardware specifications. For this reason, some T-Engine devices for development and evaluation purposes (T-Engine Appliances) have software structures including T-Kernel that comply with T-Engine specifications but hardware specifications that differ from those of standard T-Engine and μT-Engine.*1

The standard T-Engine and μT-Engine board specifications can be used as reference specifications for development and evaluation of overall hardware aspects including the physical forms of boards, connector positions, and expansion bus connectors (covered below). The standardization of standard T-Engine and μT-Engine board size and connector positions is very convenient when, for example, preparing a mockup for demonstration purposes by putting a case on a prototype developed using T-Engine. Also, products such as expansion FPGA boards and universal boards that can be used with multiple standard T-Engine and μT-Engine devices are available on the market. These have also benefited from standardization of specifications, including those for hardware, making possible such distribution of these optional hardware components.

*1: Examples include the Teacube/VR5701 evaluation kit and Teaboard2/ARM920-MX1. For more information on each of these, see: http://www.t-engine4u.com/

(2) Standard T-Engine and μT-Engine

As noted above, there are two types of specifications for T-Engine development evaluation boards: standard T-Engine and μT-Engine. Either of these can be chosen for use as appropriate for the size and purpose of the target embedded device.

Standard T-Engine is a standardized specification for development evaluation boards targeting development of devices with relatively high-level user interfaces such as GUIs using LCDs and touch panels. This standard also requires a CPU with a memory management unit (MMU). Use of an MMU promotes modularization of programs and increases the efficiency of software development for large-scale systems. The standard T-Engine hardware specifications reflect the high level of need for an MMU for supporting the running of dynamic applications such as those seen in PDAs.

On the other hand, μT-Engine is intended for devices with relatively small-scale user interfaces and used to run fixed applications for control purposes. As such, it primarily targets the type of projects that would have used ITRON in the past.

Specifications for board size and connector positions also are standardized for each of these boards. While the standard T-Engine has a CPU board size of 75 mm x 120 mm, μT-Engine has a CPU board size even more compact at 60 mm x 85 mm. Also, while the standard T-Engine has a PC card slot and USB, μT-Engine has a Compact Flash (CF) card slot as well as an MMC or SD card slot. Table 1 shows the differences between the specifications of each board.

T-Kernel, the standard real-time OS for T-Engine, runs on both standard T-Engine and μT-Engine, with no differences in specifications between the two boards. Also, since peripheral I/O differences are absorbed by device drivers, in principle higher layer middleware and applications will run on both standard T-Engine and μT-Engine. However, standard T-Engine requires an MMU while the CPU on a μT-Engine board will not necessarily have an MMU. This difference may lead to limitations on use of some middleware such as T-Kernel Standard Extension.

Table 1.1.1: Comparison of standard T-Engine with μT-Engine

	Standard T-Engine specifications	μT-Engine specifications
CPU	32 bits or more	
MMU	Required	Optional
RAM capacity	appropriate	
Flash memory capacity	appropriate	
Serial I/O	115.2kbps or faster	
Real-time clock	Y	
Audio I/O I/F	Y (IN: 1ch, OUT: 2ch)	N
eTRON Card I/F	Y	
LCD I/F	Y	N
USB Host I/F		
Expansion board I/F	Y	
Other I/F	PC Card slot (Type II) x 1 USB host x 1	CF card slot (Type II) x 1 MMC card slot x 1
Board size	75 mm x 120 mm	60 mm x 85 mm

(3) Characteristics of T-Engine hardware specifications

Specifications and functions of the standard T-Engine board and the μT-Engine board that could be considered characteristic are described below. See the relevant specifications documents for each board concerning specific specifications.

• Free implementation of CPUs and peripheral devices

Although a wide range of hardware specifications, including functions of peripheral devices, have been standardized for standard T-Engine and μT-Engine, the only required standard for the core component — the CPU — is that it be at least a 32-bit CPU. Developers have complete freedom in choosing architecture and other specifications. Actual standard T-Engine and μT-Engine boards have been developed featuring a wide range of CPUs, centered on SH, MIPS, and ARM CPUs.

Although a wide variation in CPUs can have some drawbacks in regard to standardization, since CPUs for embedded devices face a wide range of requirements such as those concerning chip cost, power consumption, and on-board peripherals in addition to architecture and performance, restricting CPUs would be difficult. Also, since in the future a great number of semiconductor companies is likely to develop a wide range of new CPUs in response to these requirements, it would not be desirable for T-Engine standardization to limit the range of CPUs that could be used.

At the same time, for the most part differences in CPUs can be absorbed in the CPU-dependent portions of compilers and T-Kernel, thus minimizing their effects on middleware and applications. This is why the T-Engine project lets developers freely choose CPUs. This can be said to reflect strongly the specific circumstances of embedded systems and is contrary to practice in the world of PCs and game consoles, in which CPUs and other hardware components are heavily standardized.

In addition, although with regard to peripheral devices functions such as USB, PCM,PC Card and CF interfaces are standardized, aspects of implementation methods such as peripheral-device control chips are not standardized. Since there are also no particular standards specified with regard to the division of roles between hardware and software (device drivers), there is no need to realize all functions using hardware. Device drivers may be used to assist in implementing functions. Still, since development of device drivers is not a simple task, it can be said that unless there are specific plans for development of a device driver it would be less troublesome to use peripheral-device control chips already used commonly in standard T-Engine and μT-Engine devices, as much as possible. Using peripheral-device control chips already used in T-Engine devices makes it possible to reduce development costs for the entire system by simplifying the device-driver porting process.

• Standardization of board specifications such as physical size, connector positions, and screw positions

As noted above, the T-Engine standard covers not just the functions of peripheral devices for the development evaluation boards but also board specifications such as physical size, connector positions, and screw positions. Although these points are not related to software compatibility, they are very convenient for aspects of development such as designing the exteriors of demonstration models, because they make it easy to share prototype cases and installation hardware.

An optional product on the market that utilizes the benefits of this standardization of specifications such as physical size is the T-Engine Development Bench.[*2] This product is a set of hardware including, among others, an acrylic stand to which the standard T-Engine board and the μT-Engine board can be attached, an LCD-board cover, a plastic board that makes it easy to carry the standard T-Engine board around, and special supports. It is very useful for purposes such as protecting boards and improving their portability and appearance. Since this product is not dependent on the model of T-Engine (or type of CPU), it can be used with all T-Engine boards, including

standard T-Engine boards and μT-Engine boards yet to be developed. This is possible because the board sizes and positions of screw holes and connectors are standardized for standard T-Engine boards and μT-Engine boards.

*2: Now under development by Personal Media Corp. See: http://www.t-engine4u.com/

• Newly developed expansion bus connector with keying (from Kyocera Elco)

Standard T-Engine and μT-Engine CPU boards feature standardized T-Engine expansion bus connectors, which can be used to stack expansion boards atop CPU boards. This expansion bus connector has a pitch of 0.5 mm and 140 pins and was developed by Kyocera Elco as a new connector for the T-Engine project. *3

*3: See: http://www.kyocera-elco.com/prdct/type/board/5603.html
This connector is available from Personal Media Corp.
See: http://www.t-engine4u.com/products/connectors.html

From the stand point of practical efficiency, the standard T-Engine and μT-Engine hardware specifications do not standardize specifications such as expansion bus connector pin arrangements, protocols, or timing, focus on practical efficiency, . As a result, such specifications vary by CPU. (Arrangements are standardized for only a very small selection of pins such as power and ground pins.)

Although standardization of physical board size also requires specification of physical forms for connectors, using the same connector with separate CPUs having different bus specifications would involve the risk of hardware damage due to possible incorrect insertion of boards. The expansion bus connector developed for T-Engine use solves this problem using different types of notch patterns in the connector housing (referred to as keying). This makes it possible to differentiate logically which individual connectors can and cannot be inserted. For example, the T-Engine/SH7751R CPU board with an SH7751R on board uses an expansion bus connector with the keying 04-01. By selecting the same keying for an expansion board for use with the T-Engine/SH7751R, it is possible to produce expansion boards that cannot be inserted into T-Engine units using CPUs other than the SH7751R.

Under this method, by not using any notches it is possible to create master expansion bus connectors that can be inserted into any connector regardless of its keying. Referred to as “00-00” keying, this connector keying is useful when building expansion boards that can be used with any CPU, such as universal boards and expansion FPGA boards. However, since as noted above such connectors are also subject to incorrect insertion, they should be used with care.

Furthermore, some expansion bus connectors use keying effectively to enable multiple specific combinations. For example, expansion bus connectors using the keying 04-00 and expansion boards using those connectors can be inserted into connectors using the pattern “04-xx” (i.e., 04-01, 04-02, etc.). In fact, a number of standard T-Engine and μT-Engine boards with PCI-compatible buses have been assigned the keying 04-XX. By setting the keying of an expansion board for connecting to a PCI-compatible bus to 04-00, it is possible to insert the boards to a T-Engine/SH7751R board with the keying 04-01 as well as to a T-Engine/Vr5701 board with the keying 04-04. (Both of these have PCI-compatible buses.)

On the other hand, different keying (01-XX, 02-XX, etc.) is assigned to T-Engine boards with no PCI-compatible buses. For this reason, an expansion boards with the keying 04-00 cannot be inserted into such a board. In this way, incorrect insertion can be prevented based on whether or not a PCI-compatible bus is used. It is also possible to build, for example, expansion boards that can be inserted into a T-Engine/SH7751R board but cannot be inserted incorrectly into a T-Engine/VR5701 board, for example by using the bus-connector keying 04-01 for an expansion board using the T-Engine/SH7751R’s local bus.

• Serial connectors and cables

Standard T-Engine and μT-Engine come with RS232C serial port for debug console during development. All models in standard T-Engine and μT-Engine family use 15-pin RMC-EA15MY-OM15-MC1 manufactured by HONDA TSUSHIN KOGYO CO., LTD., LX60-16S manufactured by HIROSE ELECTRIC CO., LTD., or the compatible products for serial port connector.

Serial cables for connecting this connector to the standard DSUB-9 connector used as a serial port on PCs and other devices appear to be provided often with products such as standard T-Engine boards and μT-Engine boards and the T-Engine Development Kit[*4] combining this hardware with software such as an OS and a development environment. From the opposite perspective, when developing and providing a standard T-Engine or μT-Engine board it might be necessary to include this serial cable in addition to an AC adapter.

*4: Available from Personal Media Corp. See: http://www.t-engine4u.com/

(4) Functions not included in standard T-Engine hardware specifications

Although T-Engine specifications cover peripheral functions needed by standard T-Engine and μT-Engine boards, these are only the minimum required functions. There would be no particular problems with adding other functions. In fact, standard T-Engine boards and μT-Engine boards with the following functions added are available on the market, with these added functions serving as the strong points of the individual products.

• VGA output connector

Makes it possible to connect the device to a PC’s LCD monitor or other device to display graphics.

• Additional serial port

Makes it possible to use a second serial port for control by applications or other use, in addition to the serial port for use with a debugging console.

• USB function

Makes it possible to use the USB function feature in addition to the USB-host feature required by standard T-Engine.

• IDE connector

Features a connector that can be connected to an IDE hard drive, making it possible to connect and use a 2.5-inch hard drive.

• LAN connector

In T-Engine, LAN connection is often realized with extension board. However, there are also standard T-Engine boards equipped with LAN connector.

• CAN and other I/Os

Enables I/Os such as CAN interfaces supported by the CPU, for use by device drivers and applications.

• Other

In some cases, minor input/output functions such as DIP switches, LED, and GPIO can be used.

In some cases, the above peripheral functions may be provided via small separate boards known by names such as connector boards and I/O boards.

(5) Specific examples of T-Engine boards, and relations with standard hardware specifications

As a summary of this chapter, Figures 1.1.2 and 1.1.3 show specific arrangements of implementation of CPUs and peripheral-device control chips, connector, etc. on a standard T-Engine board actually available on the market (T-Engine/SH7760). Table 1.1.2 shows the relationship with standard T-Engine hardware specifications. Use these for reference purposes when learning about T-Engine hardware specifications.

Table 1.1.2: Photographs of a T-Engine/SH7760 board (Figures 1.1.2 and 1.1.3) and relations with standard hardware specifications

Legend	Meaning	Specific details in T-Engine/SH7760
Solid outlines	Connector whose position and form are covered in standard T-Engine hardware specifications	Serial connector, eTRON SIM card interface (SIM connector), expansion bus connector, PC Card connector, LCD board interface, USB connector, audio connector, power connector
Dotted outlines	Connectors etc. added to this T-Engine individually and not included in standard T-Engine hardware specifications	I/O-board interface, 8-bit DIP switch
Solid underlines	Chips that are functionally required in standard T-Engine hardware specifications but whose position, installation direction, etc. are not specified	SH7760 (CPU), PC Card controller, SDRAM, flash memory
Dotted underlines	Chips implemented for realizing the functions of a CPU board, but not covered in standard T-Engine hardware specifications	H8/3048F-ONE, H8/3048F-ONE write connector, PLD

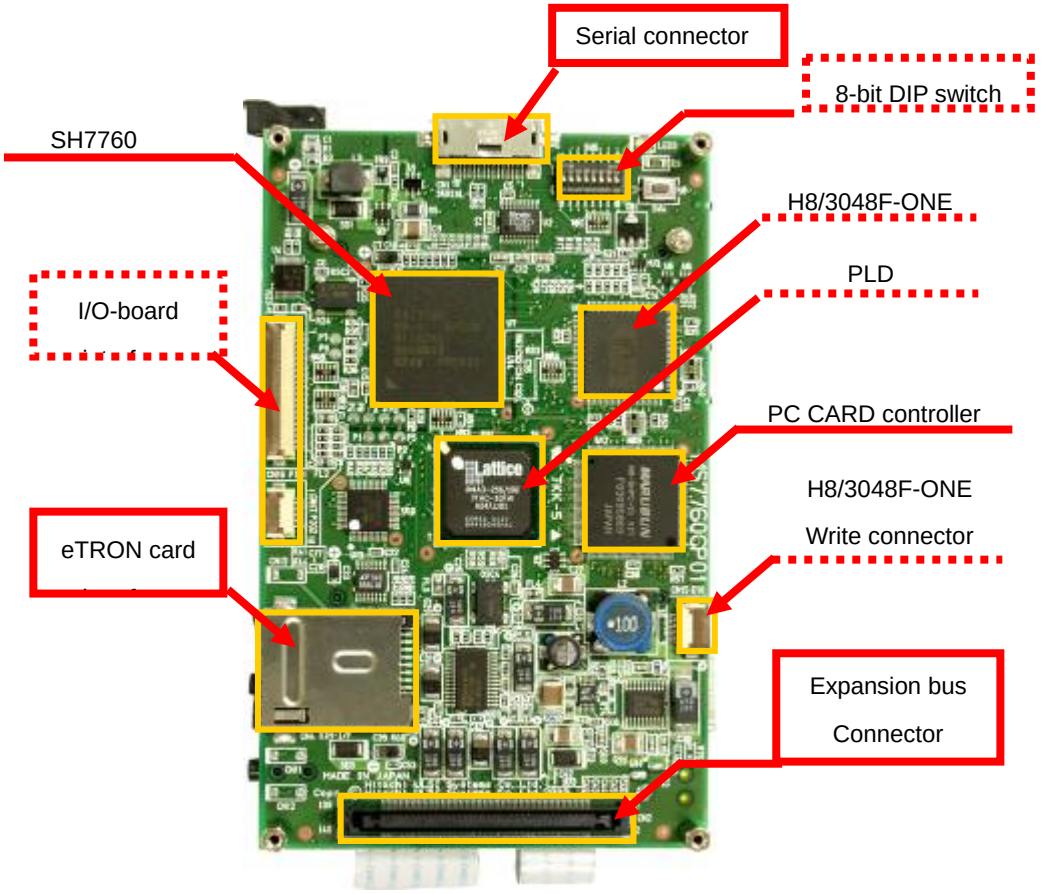


Figure 1.1.2: Photograph of T-Engine/SH7760 board, and component structure (CPU side)

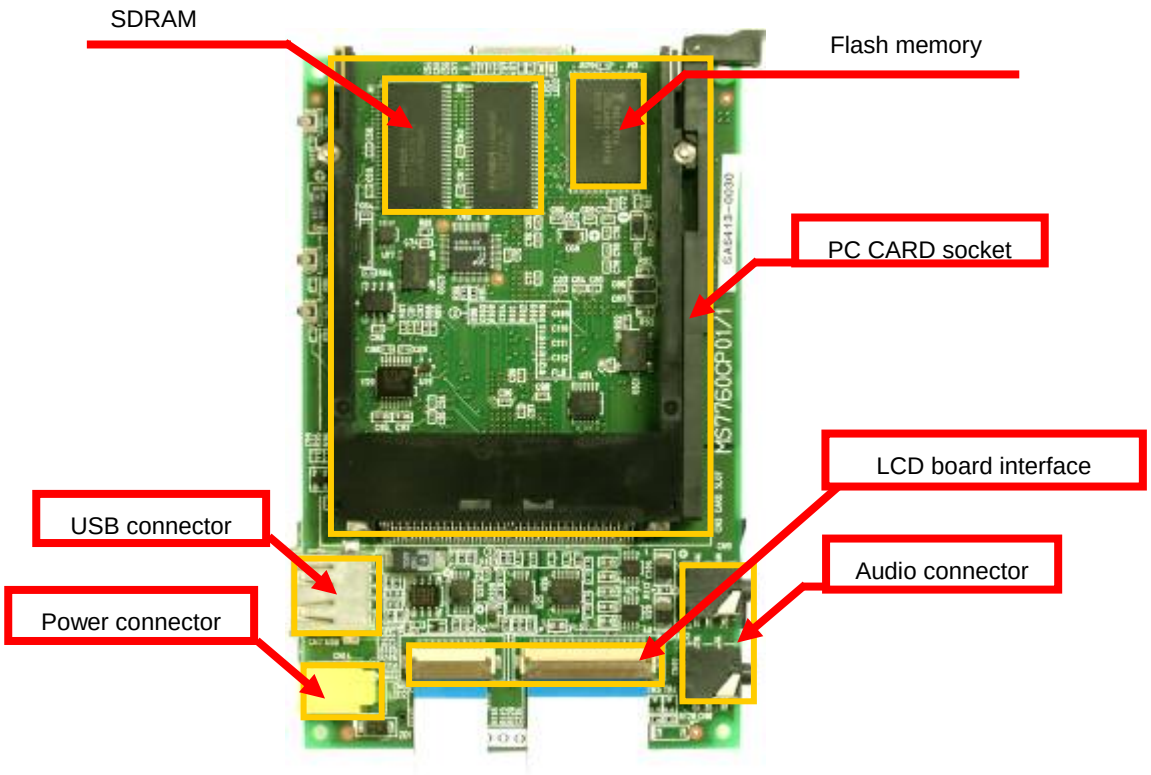


Figure 3: Photograph of T-Engine/SH7760 board, and component structure (underside)

1.2. T-Engine system structure

1.2.1. T-Engine board structure and optional products

In addition to standard T-Engine and μT-Engine CPU boards featuring a wide range of CPUs, the T-Engine lineup includes a wealth of expansion boards and optional products. The expansion boards and optional products include some that may be combined with multiple CPU boards, so that even newly developed standard T-Engine and μT-Engine CPU boards may be able to use existing expansion boards and optional products. Be sure to refer to the range of existing products when developing boards.

(1) CPU board

As of November 2007, the standard T-Engine and μT-Engine CPU boards shown in Table A1 of Appendix A either had been developed or were under development.

(2) Expansion LAN board

Since a standard T-Engine or μT-Engine CPU board does not have an on-board LAN function, a PC LAN card or an expansion LAN board must be used. Expansion LAN boards are available corresponding to the types of keying used by expansion bus connectors. Specifically, expansion LAN boards are available for use with T-Engine/SH7727 and SH7760 (keying: 01-01), with all T-Engine/ARM models (keying: 03-03), with T-Engine/SH7751R (keying: 04-01), and with T-Engine/VR and TX (keying: 04-04).

In addition, we also have models which have LAN port on connector board attached to CPU board such as T-Engine/PPC-V4FX, and models which come with LAN expansion board such as μT-Engine/M32104.

(3) LCD board

The standard T-Engine CPU board has an interface for connecting an LCD board. An LCD board with a touch panel can be connected to this interface. The LCD board can be used with all standard T-Engine models. Also, since this LCD board has a button with a “○” on it and one with an “×” on it and a directional button, it can be used for minor HMI building and testing.

In some cases (e.g., T-Engine/SH7727), an LCD board comes with the CPU board, while in other cases it must be purchased separately.

(4) Debugging board

Basically, a debugging board is used when connecting to ICE. However, some models do not require a debugging board when connecting to ICE and some require connection to ICE using a different method, and some CPU boards come together with debugging boards. Be sure to check information on the model you will use.

(5) Expansion FPGA board

Expansion FPGA boards for T-Engine use, featuring field programmable gate arrays (FPGAs) from major manufacturers Altera and Xilinx, have been developed that can be used by connecting them with (most) standard T-Engine and μT-Engine CPU boards. Using an expansion FPGA board makes it possible to develop the hardware needed by prototypes and final products even more quickly and more efficiently.

(6) Universal expansion board

So that expansion boards can be created by hand for purposes such as development, evaluation, and testing, expansion universal boards are available as options for some standard T-Engine and μT-Engine models.

Although the specialized T-Engine/μT-Engine expansion bus connector described in the next section can be used for building expansion boards for T-Engine use, since this is a 0.5-mm pitch, 140-pin connector wiring it by hand is difficult. In such a case, use of a universal expansion board is recommended.

(7) Specialized T-Engine/μT-Engine expansion bus connector

The expansion bus connector described above, developed as a new connector for the T-Engine project, is available on the market as an option for use with T-Engine. When obtaining one of these, use caution with regard to keying and plug/receptacle differentiation.

(8) T-Engine Development Bench

This product is an optional set of hardware including, among others, an acrylic stand and cover for protecting the standard T-Engine CPU board and LCD board, LCD-board buttons, and supports and screws for keeping the four corners of the boards in place.

Although T-Engine boards can be used in bare state, in consideration of factors such as ease of transporting them for demonstration and testing purposes and ease of handling, it would be desirable for the boards to be protected physically to some degree. The T-Engine Development Bench can be used for this purpose. It can be used in various ways. For example, the plastic cover can be used as a simple portable case and the thick acrylic base can be used as a stand. (See Figure 1.2.1) It can handle additional expansion boards through the addition of supports and using longer screws.

Figure 1.2.1: T-Engine Development Bench

1.2.2. T-Engine software structure

Although this document is intended primarily for hardware developers, the T-Engine software structure is described here to improve understanding of the T-Engine platform.

When starting up a T-Engine system, first of all software known as T-Monitor will start, to boot the real-time OS T-Kernel, device drivers, and other software. Refer to Figure 5 below to help understanding of the following description of the T-Engine software structure.

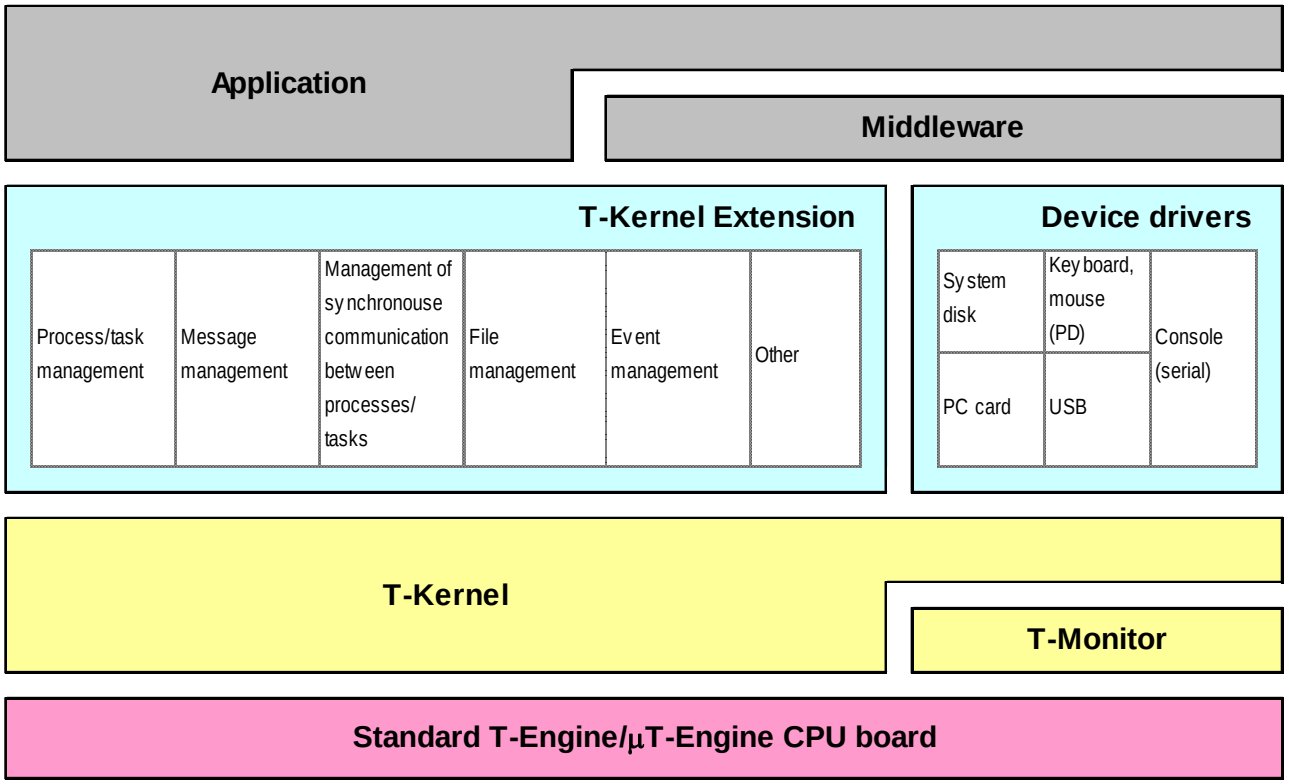


Figure 1.2.2: T-Engine software structure

(1) T-Monitor

T-Monitor runs in standard T-Engine and μT-Engine Flash ROM, handling tasks such as self-diagnosis and initialization of hardware immediately following powering the system on, booting the OS, and interactive debugging (such as memory reference and break-point configuration) under a non-OS environment. It also handles processing of some interrupts and exceptions while the OS is running. In addition, it has monitoring-service functions that run in a non-OS environment, such as input of characters to and output of characters from the console and disk access, making it usable for minor debugging. The functions of T-Monitor are similar to those of a PC's BIOS.

(2) T-Kernel

As the standard real-time OS for standard T-Engine and μT-Engine, T-Kernel is a platform for executing a wide range of middleware and applications. In addition to its basic functions as a real-time kernel similar to ITRON (T-Kernel/OS), T-Kernel has the T-Kernel/SM (System Manager) function for increasing ease of middleware distribution and the T-Kernel/DS (Debugger Support) function, which is useful for implementing software task debuggers.

To ensure more complete software compatibility, the T-Engine project has standardized the implementation of the T-Kernel real-time kernel and released its source code.

(3) T-Kernel Extension

T-Kernel Extension is middleware (basic middleware) for functional expansion of the OS, implemented using T-Kernel subsystem functions. It provides higher-level OS functions such as virtual memory using MMU, file management, and process management, and functions useful for modularization of programs.

T-Kernel Standard Extension (TKSE) is a typical example of T-Kernel Extension. The equivalent capability of UNIX kernel and its file system layer can be achieved by combining TKSE with T-Kernel. These are referred to as Ported Extensions. Examples include T-Linux, which runs Linux on T-Kernel, and T-JV, which runs Java on T-Kernel.

The combination of T-Kernel with T-Kernel Standard Extension (TKSE) makes it possible to realize functions corresponding to UNIX's kernel and file-system layers. Since implementation of TKSE requires MMU, it cannot be used on some μT-Engine platforms with no MMU.

(4) Device drivers

Device drivers make access to various peripheral devices available for general use. Since under T-Kernel the application program interface (API) used in calling device drivers from application tasks and the API used in registering new device drivers are standardized, a high level of compatibility can be ensured both for device drivers themselves and for the applications that use devices. In addition, for devices such as serial ports and system disks (CF/MMC cards) that come with or can be connected to standard T-Engine boards and μT-Engine boards, functions dependent on individual devices are also standardized.

T-Engine device drivers can also be loaded dynamically. In other words, there is no need to link all drivers when

building a system or to load all drivers in advance when starting up a system. Rather, new drivers can be loaded and executed while the system is running. Used property, this function enables functions like the “plug and play” functions of a PC and live insertion and removal of peripheral boards. This function is especially useful for devices such as PC cards and USB peripherals, with hardware compatible with live insertion and removal.

(5) Other middleware

A wide range of middleware has been implemented at an even higher level than T-Kernel and T-Kernel Extension. For example, the PMC T-Shell[*5] GUI middleware handles GUI-related processing, such as rendering of images and text to the screen and management of windows and components. Also, a number of high-level functions have been implemented as applications running on PMC T-Shell. These include implementation of the simple scripting language known as Microscript and an HTML browser. This middleware is useful for increasing the efficiency of developing embedded systems including GUIs.

*5: See: http://www.t-engine4u.com/

■ Chapter 2: CPU-board design methods

2.1. CPU

Standard T-Engine specifications require a 32-bit or higher CPU with a memory management unit (MMU) on board. While μT-Engine specifications require a 32-bit CPU, the MMU is optional.

Existing standard T-Engine and μT-Engine boards feature the following CPUs:

(as of June 2009)

[Standard T-Engine]

CPU	Details	Manufacturer
SH7727	SH3-DSP Core, 96 MHz	RenesasTechnology
SH7720	SH3-DSP Core, 133 MHZ	
SH7751R	SH-4 Core, 240 MHz	
SH7760	SH-4 Core, 200 MHz	
SH7780	SH-4A Core, 400 MHz	
VR5500A	MIPS Core, 400 MHz	NEC Electronics
VR5701A	MIPS Core, 333 MHz	
TX4956	MIPS Core, 400 MHz	Toshiba
ARM720-LH7	ARM720T Core, 77.4 MHz	NXP
ARM922-LH7	ARM922T Core, 200 MHz	
ARM926-MB8	ARM926EJ-S Core +ARM946E-S Core, 200 MHz	Fujitsu MicroElectoronics
ARM926-MX21	i.MX21, ARM926EJ-S Core, 266 MHz	Freescale
ARM920-MX1	i.MX1, ARM920T Core, 200 MHz	
PowerPC	PPC-V4FX Core, 300MHz	XILINX

[μT-Engine]

CPU	Details	Manufacturer
SH7145	SH2 Core, 50 MHz	Renesas
M32104	M32R Core, 216 MHZ	
M32192	M32R-FPU Core, 160 MHz	
V850E/MA3	V850E1 Core, 80 MHz	NEC Electronics
VR4131	MIPS Core, 200 MHz	
Nios Ⅱ	32-bit RISC	Altera
ARM7-LH79532	ARM7TDMI Core, 50 MHz	NXP

2.2. Memory (Flash Memory, RAM)

With regard to memory, specifications do not include requirements for types or capacities of ROM or RAM. Memory size is determined by the needs of the CPU and applications used.

Existing standard T-Engine and μT-Engine boards feature the following memory configurations:

[Standard T-Engine]

CPU	ROM	RAM
SH7727	8 MB (Flash Memory)	32 MB (SDRAM)
SH7720	8 MB (Flash Memory)	64 MB (SDRAM)
SH7751R	8 MB (Flash Memory)	64 MB (SDRAM)
SH7760	8 MB (Flash Memory)	64 MB (SDRAM)
SH7780	16 MB (Flash Memory)	128 MB (DDR-SDRAM)
VR5500A	16 MB (Flash Memory)	128 MB (SDRAM)
VR5701A	16 MB (Flash Memory)	128 MB (DDR-SDRAM)
TX4956	16 MB (Flash Memory)	128 MB (SDRAM)
ARM720-LH7	8 MB (Flash Memory)	32 MB (SDRAM)
ARM922-LH7	8 MB (Flash Memory)	32 MB (SDRAM)
ARM926-MB8	16 MB (Flash Memory)	64 MB (SDRAM)
ARM926-MX21	16 MB (Flash Memory)	64 MB (SDRAM)
ARM920-MX1	16 MB (Flash Memory)	64 MB (SDRAM)
PPC-V4FX	16 MB (Flash Memory)	128 MB (SDRAM)

[μT-Engine]

CPU	ROM	RAM
SH7145	256 KB (On board) + 1 MB (Flash Memory)	8 KB (On board) + 1 MB (SRAM)
M32104	4 MB (Flash Memory)	64 KB (On board) + 16 MB (SDRAM)
M32192	1 MB (On board)	176 KB (On board) + 1 MB (SRAM)
V850E/MA3	512 KB (On board)	32 KB (On board) + 8 MB (SDRAM)
VR4131	16 MB (Flash Memory)	32 MB (SDRAM)
Nios II	4 MB (Flash Memory)	16 MB (SDRAM)
ARM7-LH79532	4 MB (Flash Memory)	16 MB (SDRAM)

■ Chapter 3 CPU-board implementation

CPU-board specifications include requirements for board size (120 mm x 75 mm), board thickness (1.6 mm), connector-position tolerance (+/- 2 mm), and hole-position tolerance (+/- 0.3 mm). They also cover the implementation and hole positions for the following types of connectors and switches.

Readers are referred to the T-Engine Hardware Specifications (TEF010-S001-01.01.02/en) for the details of implementation specifications.

[Standard T-Engine:]

1) eTRON SIM card connector
2) PC Card slot
3) USB HOST connector
4) Serial connector
5) Power switch
6) Reset switch
7) NMI switch
8) Expansion bus connector
9) Power connector
10) Headset connector
11) Headphone output connector
12) Hole positions at four Corners
13) LCD connector

[μT-Engine]

1) eTRON SIM card connector
2) Compact Flash card connector
3) MMC connector
4) Serial connector
5) Power switch
6) Reset switch
7) Expansion bus connector
8) Hole positions at four Corners

Since positions are specified for a large number of components, sufficient consideration is required concerning reducing the number of components and component layout. Although the height of components is not covered in specifications, since a T-Engine expansion board connects to the CPU board by stacking, care is also required concerning the height of components used on the CPU board.

■ Chapter 4 CPU-board interface circuitry design

4.1. Expansion bus connector design

4.1.1. Basic concept

Standard T-Engine and μT-Engine (hereinafter, except as specified otherwise these are both referred to as "T-Engine") have the minimum required interfaces for developing programs, in a compact size easy to embed in prototype devices. For this reason, in general the required input/output interfaces, peripheral LSIs, etc. are included on expansion boards that connect to the T-Engine board. The T-Engine board has connectors (expansion bus connectors) for expansion boards and for exchanging signals and power supplies. Primarily, specifications are defined for the following matters related to these connectors:

- Connector type (size, number of pins, etc.)
- Connector installation position
- Power supply pin position (four-pin only) and voltage
- Ground pin position (four-pin only)

In this way, although aspects other than those listed above (in particular, signal specifications) are not standardized, in consideration of convenience to the T-Engine user efforts have been made to ensure the sharing of such aspects as much as possible. As a result, these can be categorized into a number of groups of shared signal specifications. When developing a new T-Engine, it could be considered desirable to ascertain the latest circumstances with regard to these matters and to conform to existing specifications as much as possible.

4.1.2 Types of expansion buses (signal specifications)

[Ground and power supply]

The four pins nos. 137 - 140 are assigned as ground pins, and the four pins nos. 133 - 136 are assigned as power supply pins for power supplied from the expansion board to the T-Engine board. Power supply voltage is specified at 5V +/-5%. For this reason, the T-Engine board is designed to run over a broader range than 5V +/-5%.

The T-Engine board also has a power connector for use when using the board alone. Under the basic specifications, when connecting an expansion board, power is not supplied to the main board's power connector. Rather, power is supplied only from the expansion board side. However, it is anticipated that under actual conditions of use power might be supplied from the main board side mistakenly, damaging both the expansion board and the main board. It would be desirable to use countermeasures such as inserting a diode on the T-Engine board side.

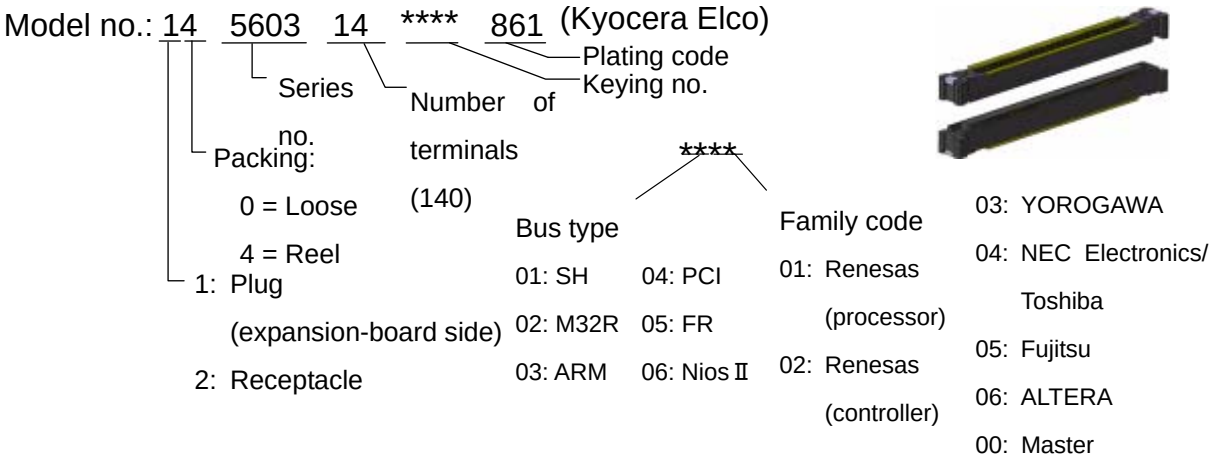
The four power supply pins are referred to as VBAT. This name is a relic of the fact that its design initially assumed power would be supplied from a secondary battery.

[Groups]

Figure 4.1.1 shows an overview of the T-Engine expansion bus connector. See Appendix B (T-Engine Expansion bus connector Signal List) concerning assignment of expansion bus connector signals. Complying with existing types as much as possible not only makes it possible to use various existing expansion boards but also can lead to reduced development costs by eliminating the need to ask the manufacturer to supply a connector with a new key. In particular, T-Engine boards with PCI buses currently have been standardized on the 04-XX type.

In addition, even when it is difficult to match signal specifications with any existing type, an FPGA board can be connected without using a converter board simply by matching the ground pin to an existing board.

Note that Figure 4.1.1 and Appendix B are subject to change without notice and that the accuracy of their content is not guaranteed.



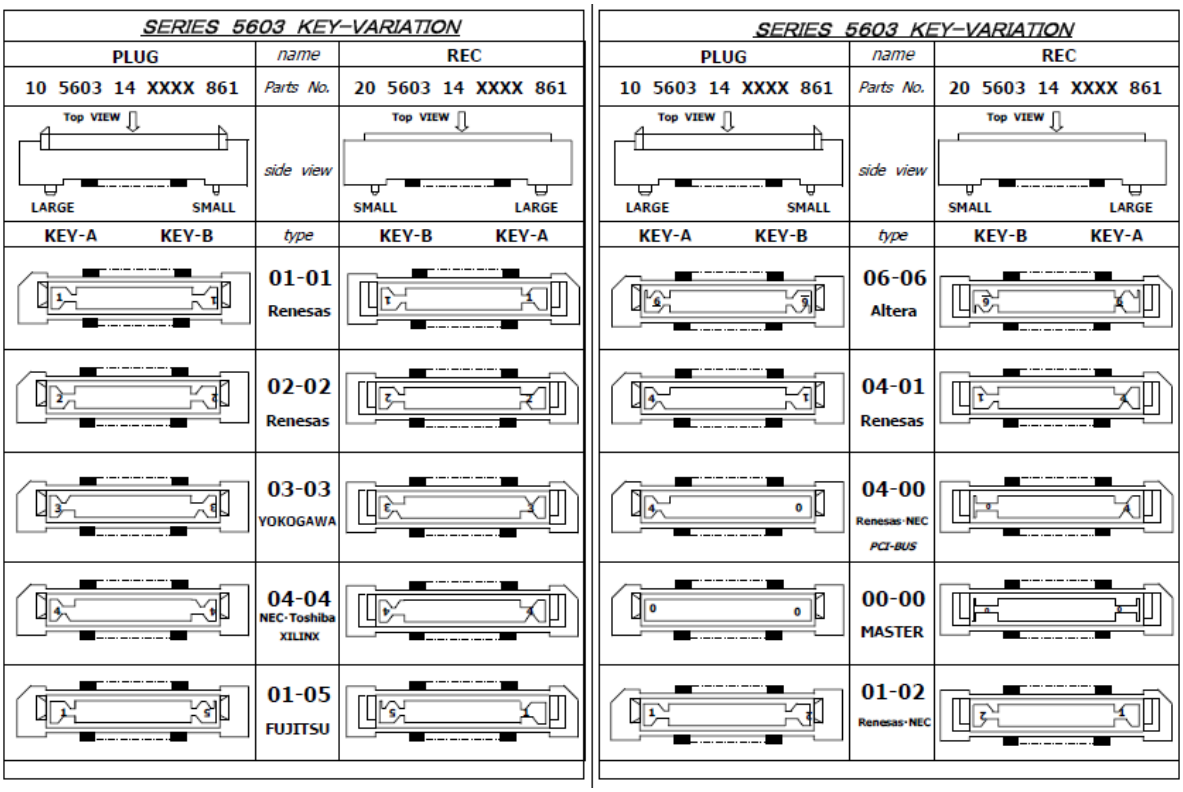


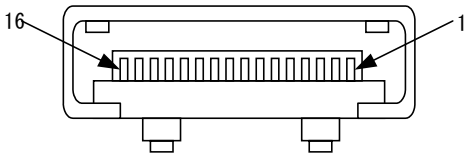
Figure 4.1.1: Keying allocation to prevent incorrect insertion of expansion bus connector.

4.2. Serial interface

A serial interface is used primarily as a debugging console port for connection with a PC. In light of installation space requirements on a T-Engine board, the following compact 15-pin or 16-pin serial connectors are recommended. For this reason, a development kit will usually supply a D-sub-9 (female) cable for connection to a PC.

15-pin serial connector
Model: RMC-EA15MY-OM15-MC1
Manufacturer: Honda Tsushin Kogyo

Pin No.	Signal
1	GND
2	TxD
3	RxD
4	GND
5	RTS
6	CTS
7	GND
8	Reserved
9	Reserved
10	Reserved
11	Reserved
12	Reserved
13	Reserved
14	Reserved
15	Reserved



16-pin serial connector
Model: LX60-16S
Manufacturer: Hirose Electric

Pin No.	Signal
1	GND
2	TxD
3	RxD
4	GND
5	RTS
6	CTS
7	GND
8	Reserved
9	Reserved
10	Reserved
11	Reserved
12	Reserved
13	Reserved
14	Reserved
15	Reserved
16	Reserved

Figure 4.2.1: Overview of recommended connector, and signal requirements

Signal lines comply with the RS-232C standard. An example of drive circuitry is shown in Figure 4.2.2.

To send and receive data in accordance with the counterpart's status, use circuitry in which the RTS/CTS and DTR/DSR signals are linked to each other.

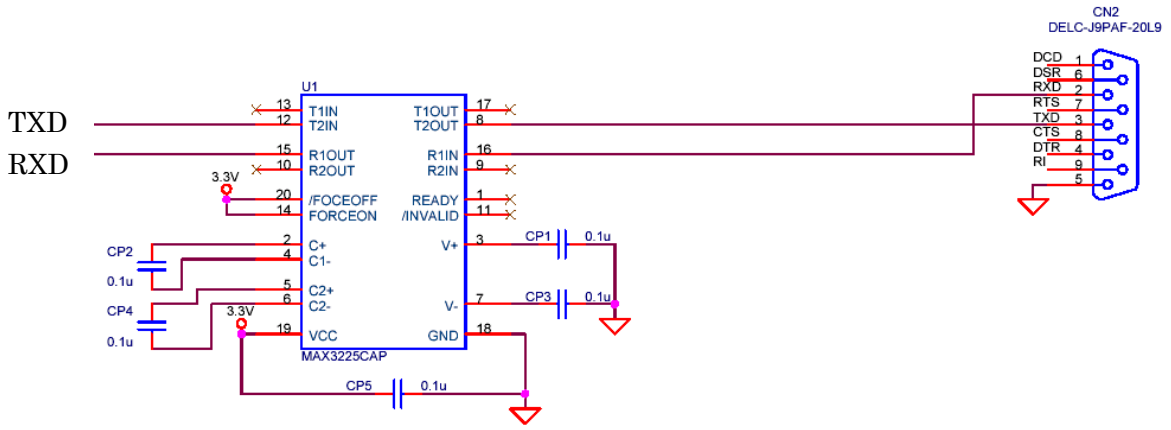


Figure 4.2.2: RS-232C drive circuitry example (from VR5500 T-Engine)

- The baud rate clock circuitry is designed to enable selection of standard speeds from 38.4 to 115.2 Kbps.

4.3. PC card interface

The board uses a single Type-II PC card slot with a 68-pin connector, compliant with the PCMCIA Rel.2.1/JEIDA Ver. 4.2 standard. When a card bus — the PC Card Standard for high-speed processing — is needed, the board shall comply with the card bus standard. Three types of spaces — attribute space, memory space, and I/O space — are used. Memory space and I/O space come in two types: 16-bit-access space and 8-bit-access space. Either of these may be chosen in accordance with access method.

Card voltage specifications are 5 V/3.3 V. A power management feature can be used to detect excess power and shut it down, using power supply control circuitry. Card detection and interrupt signals including card interrupts are interfaced to the CPU.

A recommended 68-pin connector is type no. 31-5027-068-130-833+ (from Kyocera Elco).

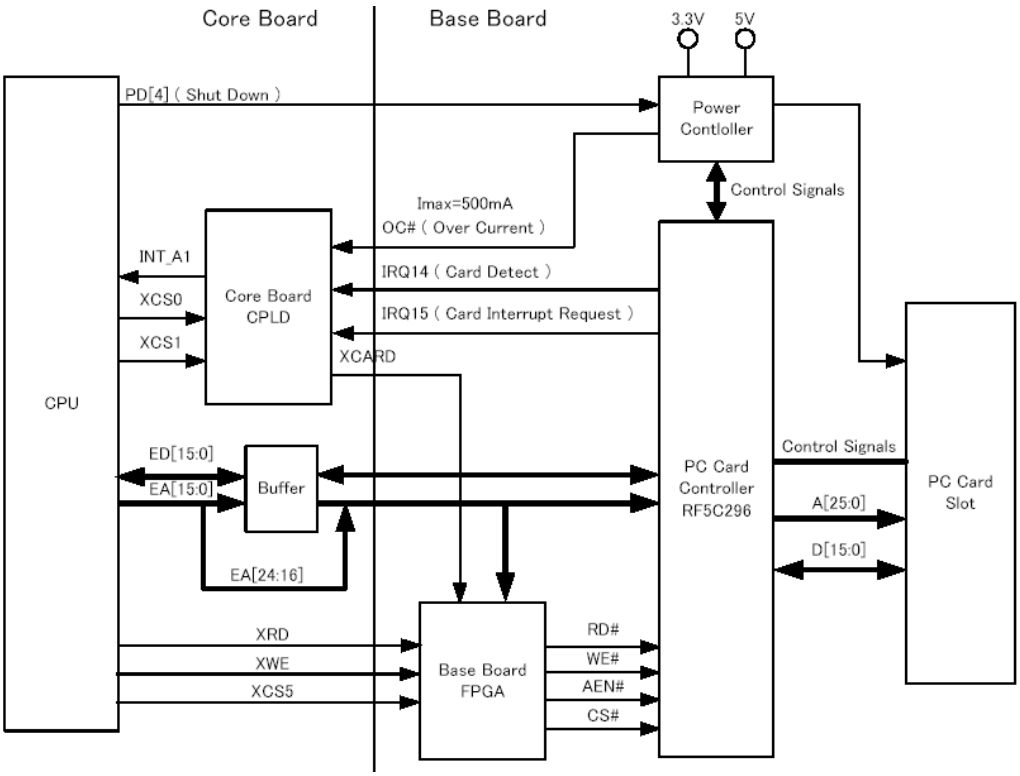


Figure 4.3.1: PC card interface circuitry structure example (from ARM926 T-Engine)

4.4. LCD/Touch panel interface

The LCD board shown below, supplied by Renesas, is recommended as the de facto standard T-Engine LCD/touch panel interface. The following figure shows a sample structure.

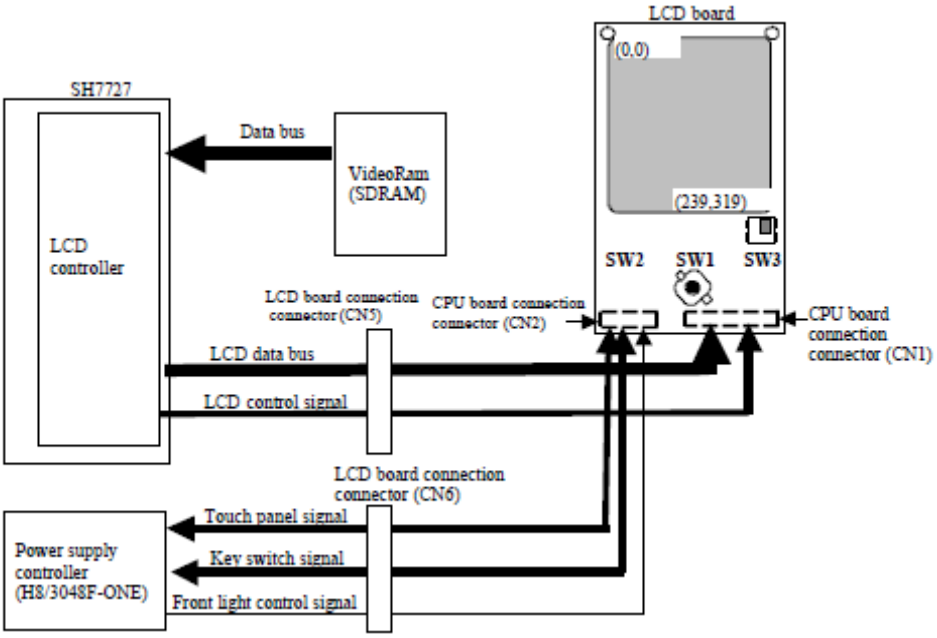
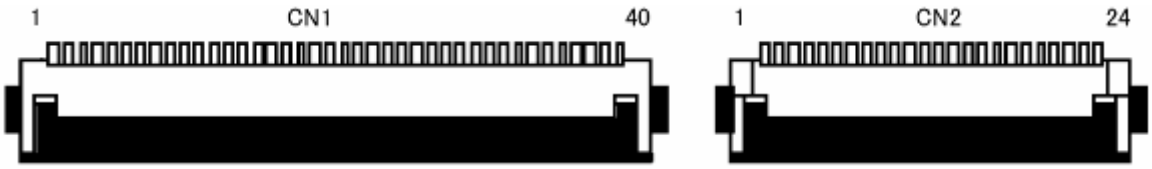


Figure 4.4.1: Example of connection between LCD board and T-Engine (example using SH7727 T-Engine)

Recommended connector specifications and signal arrangements are shown below.

1) Connector specifications:



CN1 LCD interface connector
Model: FH12-40S-0.5SH
Manufacturer: Hirose Denki

CN2 LCD interface connector
Model: FH12-24S-0.5SH
Manufacturer: Hirose Denki

2) Signal arrangement

CN1 pin arrangement

Pin No.	Signal	I/O	Notes	Pin No.	Signal	I/O	Notes
1	VBAT	-	Power supply	21	LCD13	OUT	LCDC
2	VBAT	-	Power supply	22	LCD14	OUT	LCDC
3	VBAT	-	Power supply	23	LCD15	OUT	LCDC
4	VBAT	-	Power supply	24	GND	-	Power supply
5	NC	―	Unused	25	GND	-	Power supply
6	LCD0	OUT	LCDC	26	CL1	OUT	LCDC
7	LCD1	OUT	LCDC	27	CL2	OUT	LCDC
8	LCD2	OUT	LCDC	28	DON	OUT	LCDC
9	LCD3	OUT	LCDC	29	M_DISP	OUT	LCDC
10	LCD4	OUT	LCDC	30	FLM	OUT	LCDC
11	LCD5	OUT	LCDC	31	VEPWC	OUT	LCDC
12	LCD6	OUT	LCDC	32	VCPWC	OUT	LCDC
13	LCD7	OUT	LCDC	33	NC	―	Unused
14	GND	―	Power supply	34	GND	-	Power supply
15	GND	―	Power supply	35	GND	-	Power supply
16	LCD8	OUT	LCDC	36	IR_IN	IN	Remote controller
17	LCD9	OUT	LCDC	37	3.3V	-	Power supply
18	LCD10	OUT	LCDC	38	3.3V	-	Power supply
19	LCD11	OUT	LCDC	39	3.3V	-	Power supply
20	LCD12	OUT	LCDC	40	3.3V	-	Power supply

* Leave NC and reserved terminals open on the circuit board.

CN2 pin arrangement

Pin No.	Signal	I/O	Notes	Pin No.	Signal	I/O	Notes
1	GND	―	Power supply	13	~PAD_CS	OUT	PAD_I/F
2	GND	―	Power supply	14	~PAD_IRQ	IN	PAD_I/F
3	KEY_IN0	IN	KEY_I/F	15	PAD_DIN	OUT	PAD_I/F
4	KEY_IN1	IN	KEY_I/F	16	PAD_DOUT	IN	PAD_I/F
5	KEY_IN2	IN	KEY_I/F	17	PAD_DCLK	OUT	PAD_I/F
6	KEY_IN3	IN	KEY_I/F	18	~RESET	OUT	Reset
7	KEY_IN4	IN	KEY_I/F	19	~LCD_FLON	OUT	LCD Power supply
8	KEY_OUT0	OUT	KEY_I/F	20	~LCD_PWRDY	IN	LCD Power supply
9	KEY_OUT1	OUT	KEY_I/F	21	GND	―	Power supply
10	KEY_OUT2	OUT	KEY_I/F	22	GND	―	Power supply
11	GND	―	Power supply	23	3.3VSB	-	Power supply
12	GND	―	Power supply	24	3.3VSB	-	Power supply

4.5. eTRON SIM card interface

Basically, eTRON SIM card interface specifications comply with ISO7816-1 - 3 (SIM). The T=1 protocol is recommended. The T=0 protocol is required at a minimum.

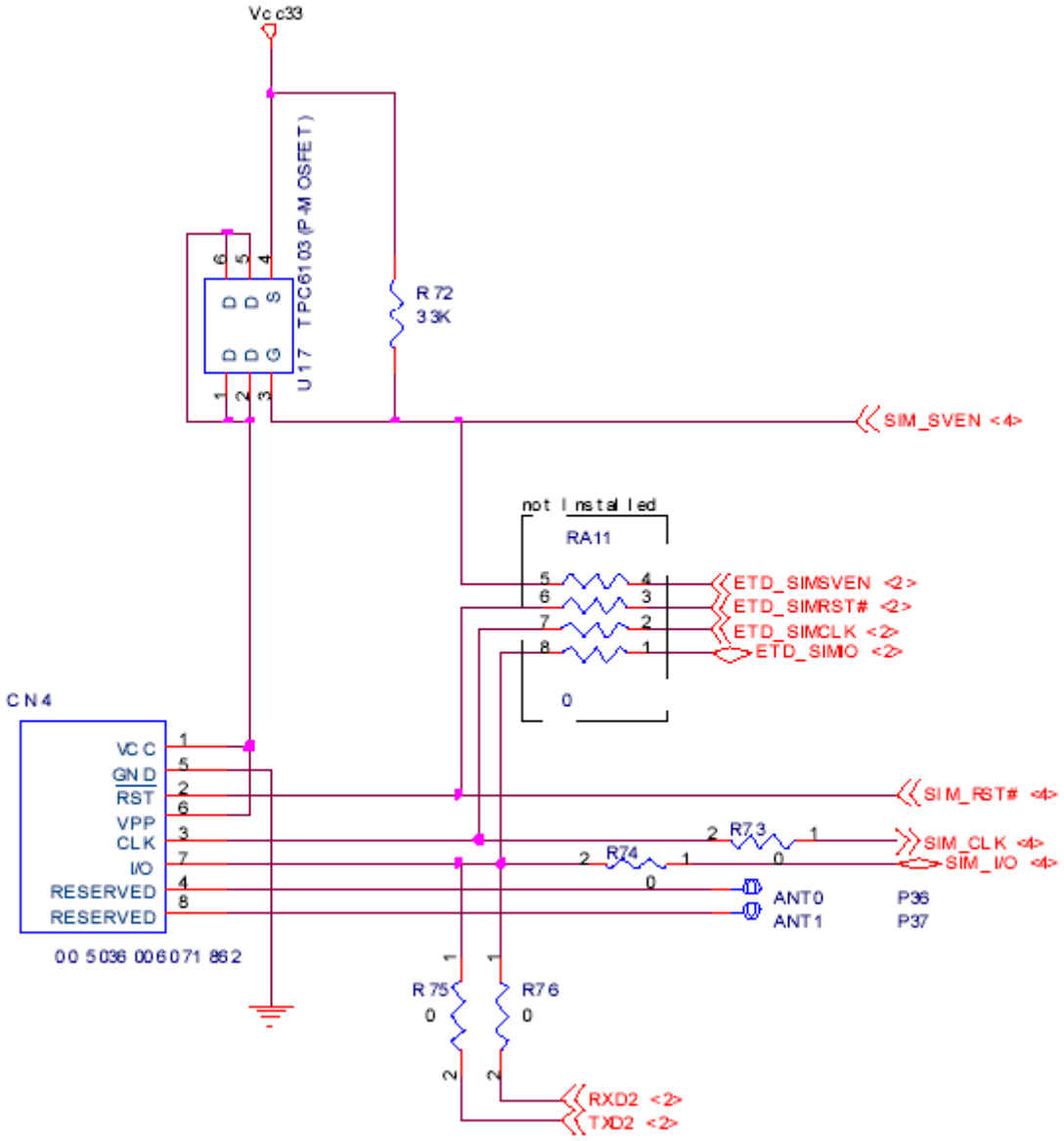
As a connector, the 04-5036-008-110-862 SIM card connector (from Kyocera Elco), which is compatible with the ETSI TS 102221 V4.1.0 VICC-Terminal Interface standard, is recommended.

PIN No	Signal	I/O	Function
1	Vcc 3.3 V	-	Power supply: 3.3 V
2	Reset	O	Reset
3	Clock	O	Clock*
4	Reserved		-
5	GND	-	Ground
6	Vpp	-	NC
7	I/O	I/O	Serial input/output
8	Reserved		-

* Supplied clock

3.5712 MHz Duty: 50±10%

Figure 4.5.1: eTRON SIM connector signals



- The circuitry above is capable of on/off control of the 3.3-V power supply.
- Handle the reserve pins (4, 8) so that they can be connected to on the printed circuit board as terminals.

Figure 4.5.2: Example of eTRON SIM Card interface circuitry (from ARM926 T-Engine)

- Cautions

(1) Power terminal control:
Since switching between the contact and contactless interface is connected based on whether Vcc power is supplied, a function for shutting of the Vcc power supply is required.

(2) Processing signals from pins 4 and 8:
When using a contactless eTRON SIM card interface, use these pins as terminals for connecting an antenna. Design throughholes near the SIM card connector to enable connection to these terminals.

(3) Power sequence:
Figure 4.5.3 shows concerning reset, clock, and power timing.

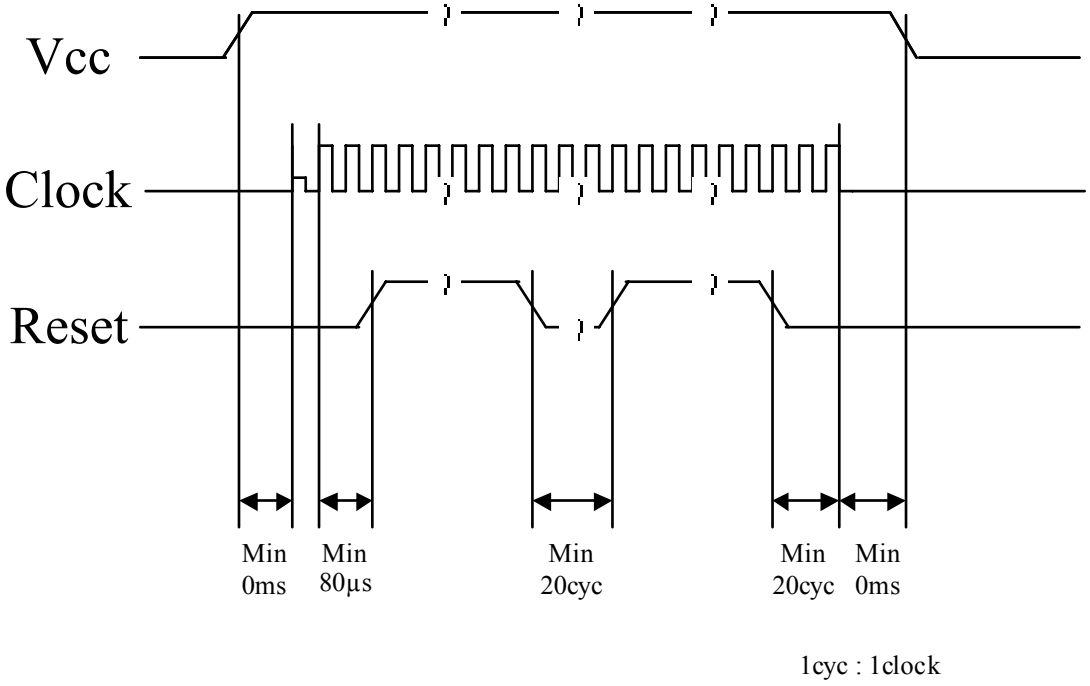


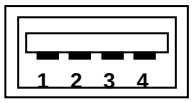
Figure 4.5.3: Power sequence

4.6. USB host interface

This interface complies with the USB Host Ver. 1.1 (12 M/1.5 Mbps) standard.

If the capacity is available on the T-Engine side's power supply, bus power can be employed to provide a power supply to connected USB devices (max. 5 V/500 mA).

A recommended connector is model no. 20-5041-004-100-834+ (from Kyocera Elco).



Pin No.	Signal	Input/output	Function
1	Vcc	—	Power supply
2	-Data	I/O	- data signals
3	+Data	I/O	+ data signals
4	GND	—	Ground

Figure 4.6.1: Connector signal arrangement

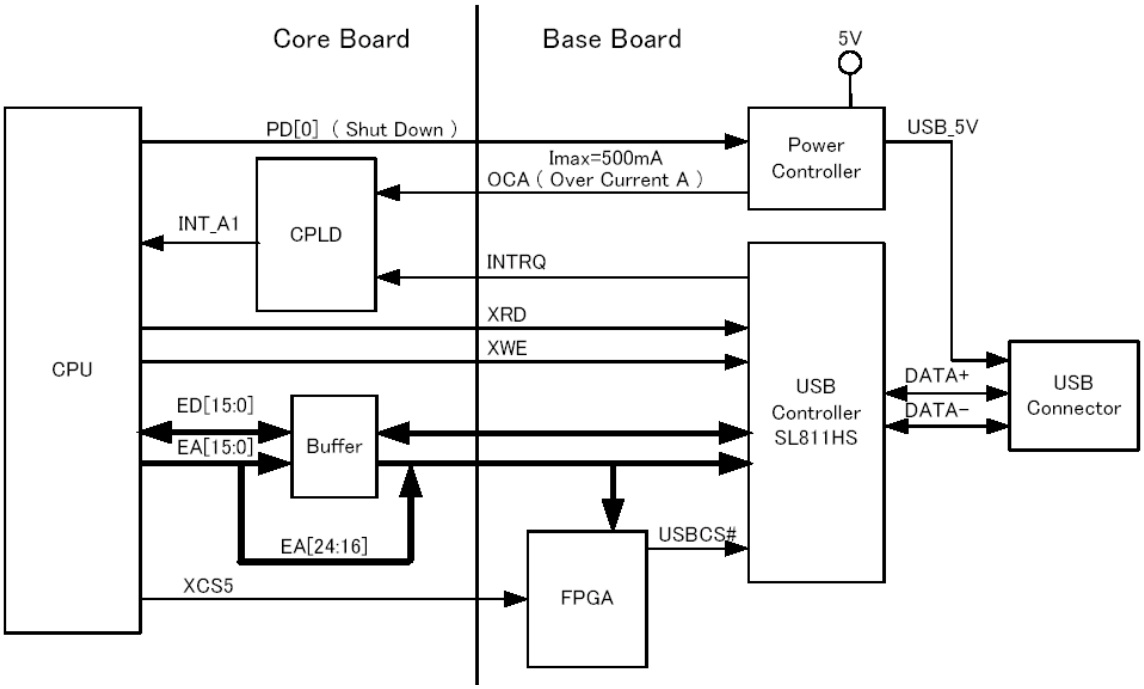
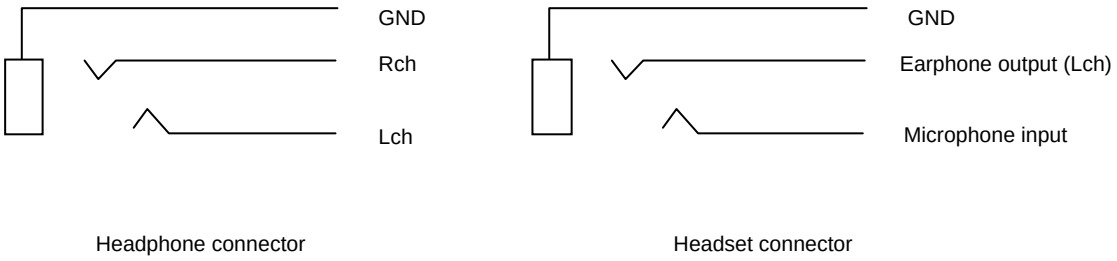
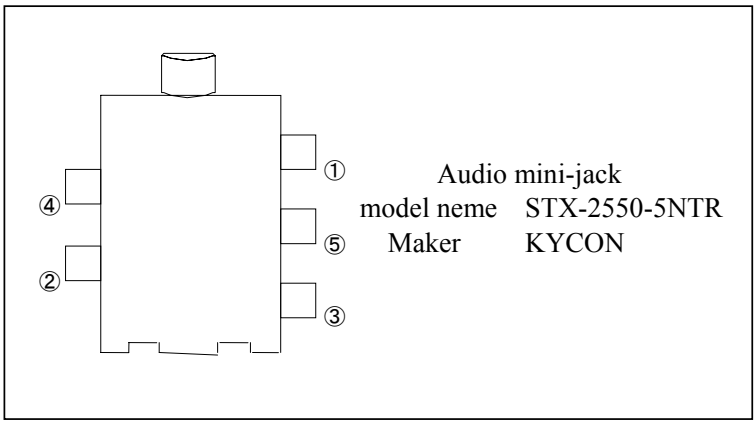


Figure 4.6.2: Example of USB interface circuitry
(from ARM926 T-Engine)

4.7. Audio input/output interface

The T-Engine hardware specifications call for signal lines with jacks 2.5 mm in diameter for audio input (monaural) and output (stereo), as shown in the Figure 4.7.1. A recommended connector is model no. HSJ1602-010011 (from Hosiden) and STX-25505NTR (from KYCON). Connect an earphone/microphone output (Lch) to enable use of headsets such as those used with mobile phones.





Pin No	Signal Name
1	GND
2	R-IN
3	R-OUT
4	MIC-IN
5	HP_SENSE

Figure 4.7.1:Audio input/output interface

Pin No	Signal Name
1	GND
2	L-OUT
3	R-OUT
4	HP_SENSE
5	NC

Figure 4.7.2:Audio output interface

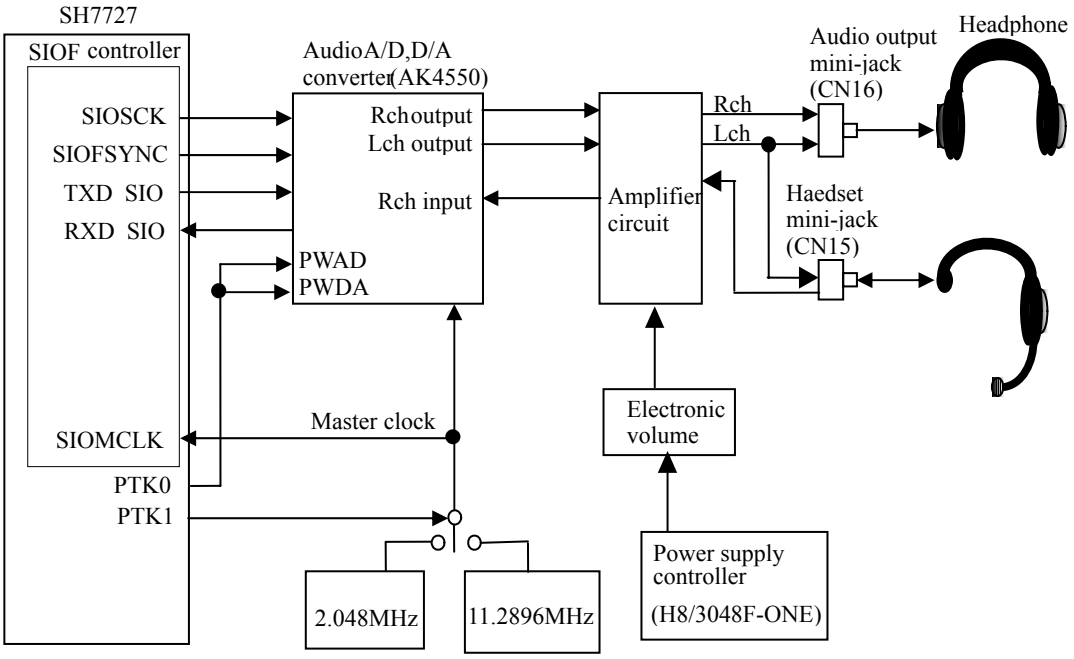


Figure 4.7.3: Example of Audio interface structure (from SH7727 T-Engine)

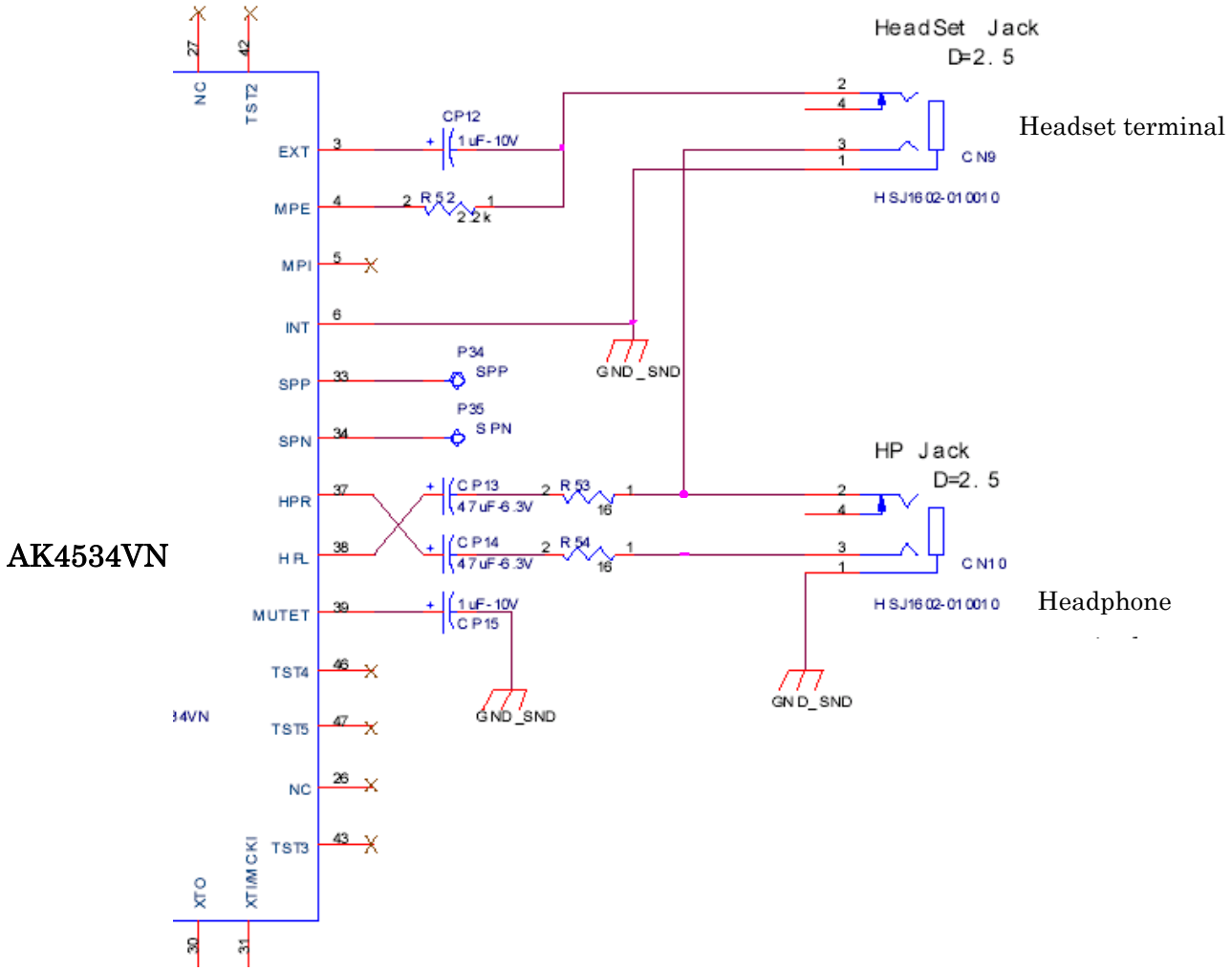


Figure 4.7.4: Example of actual circuitry (from ARM926 T-Engine)

4.8. Compact Flash card interface (µT-Engine only)

One Type-II Compact Flash (CF) card slot with a 50-pin connector is used.
A recommended connector is model no. 31-5620-050-716-833+ (from Kyocera Elco).
Interrupt signals are processed to enable hot insertion and removal. Use a power supply voltage of +3.3 V.

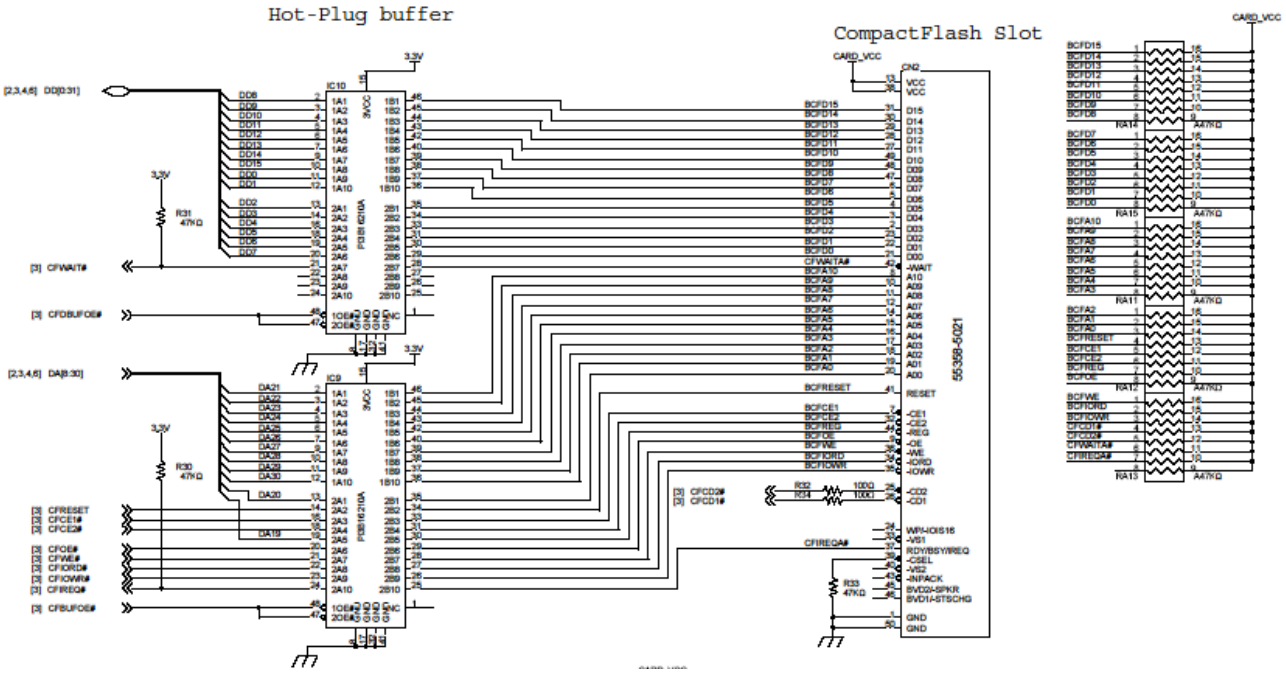


Figure 4.8.1: Example of Compact Flash card interface circuitry
(from M32104 µT-Engine)

4.9. MMC/SD card interface (µT-Engine only)

µT-Engine hardware specifications cover MMC- or SD-card connector specifications.
Interrupt signals are processed to enable hot insertion and removal. Use a power supply voltage of +3.3 V only.

- Connector specifications:
  One nine-pin slot (compatible with cards 2.1 mm thick)
  A recommended connector is model no. 10-5738-009-783-862+ (from Kyocera Elco).

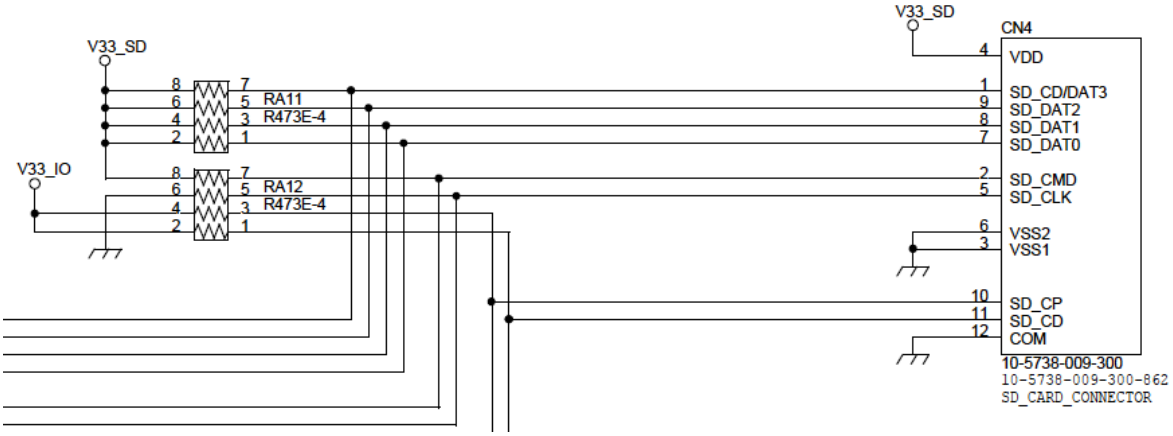


Figure 4.9.1: Example of MMC/SD card interface circuitry
(from VR4131 µT-Engine)

4.10. Power supply interface

4.10.1. Direction of power supply

Figure 4.10.1 shows a power supply diagram. The VBAT terminal (133 - 136 pins) on the expansion bus connector supplies power from the expansion board to the CPU board (T-Engine). Other power terminals supply power from the CPU board to the expansion board. For this reason, refer to the Figure 4.10.1 concerning use of diodes to prevent reverse current when inserting devices to the power circuit. For external power supply input, a connector complying with EIAJ RC5320A specifications is implemented. Voltage category 2 (3.15 - 6.3 V) is used, with negative external polarity and positive internal polarity.

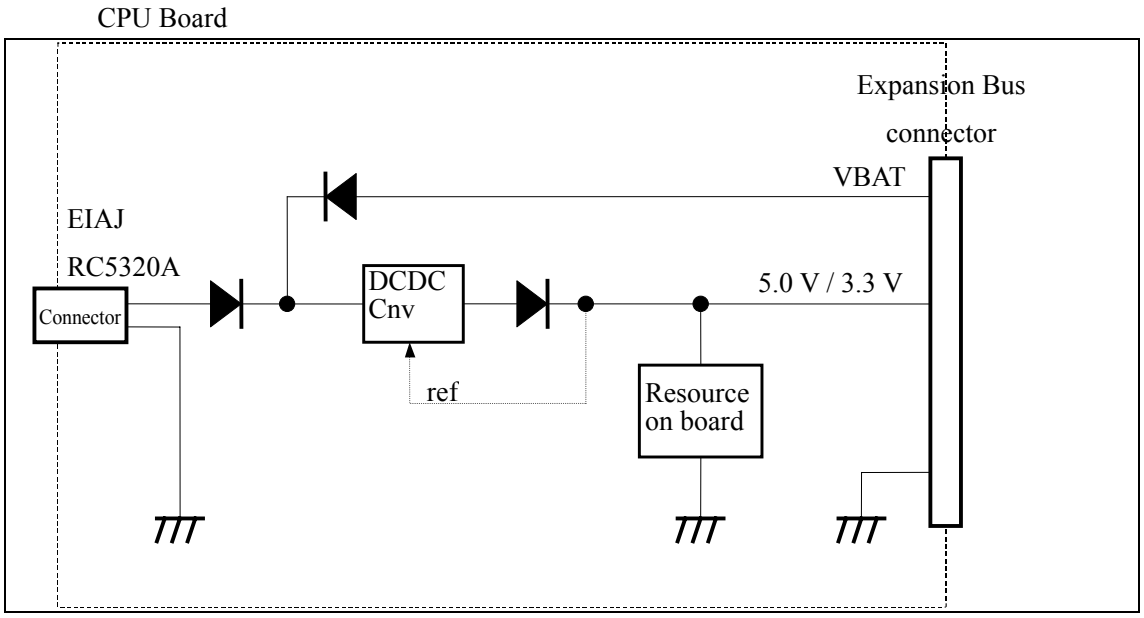


Figure 4.10.1: Direction of power supply on the CPU board (T-Engine)

4.10.2 Power state names

Under T-Engine specifications, the following names are used to manage power states. Use of the following names is recommended when designing features such as power management transition-state charts.

Name: P0
State: Main power off

Name: P1
State: Main power on, CPU in sleep mode (can be restarted by interrupt signal), memory not retained, peripheral modules optional

Name: P2
State: Main power on, CPU in sleep mode (can be restarted by interrupt signal), memory retained, peripheral modules optional

Name: P3
State: Main power on, CPU running, memory retained, peripheral modules optional

The specifications also include a more detailed naming method for sub-states of state P3, in which the CPU is

running. Under this method, the CPU's lowest operating clock-speed setting is given the suffix "1" and its highest operating clock-speed setting the highest suffix.

Ex.: Low speed: P3-1
Medium speed: P3-2
High speed: P3-3

4.10.3. Implementation of power management specifications

T-Engine hardware specifications prescribe the following external power supply control specifications. Implement power management using a power supply controller LSI or similar device.

• External power supply control function

1) Controls for turning power on
The following two types of controls for turning the power on are supported:
- Power turned on with power supply
- Power turned on using power switch

It is possible to use a DIP switch or other means to switch between the mode in which the power is turned on with a power supply and the mode in which the power is turned on using a power switch.

Furthermore, it is recommended that controlling turning the power on using power control signals on the expansion bus be supported.

Control of turning the power on using power control signals on the expansion bus should enable expansion boards with functions such as wake on LAN to control the power supply through input of power control signals.

2) Controls for turning power off
- Turning the power off using a power switch
- Turning the power off using other control commands (software control)

• Handling power failures

It is recommended that a T-Engine board have the following functions for handling power

1) Using a backup power supply (such as UPS or a battery) to detect power failures
Any of the following three types of methods may be chosen for implementing detection of power failures using a backup power supply:
- A terminal on the CPU board for input of power failure notification signals
- A function for detecting drops in battery voltage (when using a battery)
- A terminal on the expansion board for input of power failure notification signals, which would then be communicated to the CPU

2) Using nonvolatile memory, an RTC internal register, or similar means to detect power failures
A function for backing up data (such as on-board nonvolatile memory) is optional.

Figure 4.10.2 shows an example of a specific power supply block diagram.
Current restrictions and an on/off switch have been added to the power supply to peripheral devices.
Power on/off control is implemented using PD[0] - PD[4], and INT_A1 is used to send an interrupt signal when excess power has been detected.
In addition, an optional battery board can be connected, and power can also be supplied from the expansion bus connector's VBAT.

When power is supplied from the DC jack, no power is supplied from the VBAT.
Since DC_IN must exceed VBAT, care is required when selecting an AC adapter to use.

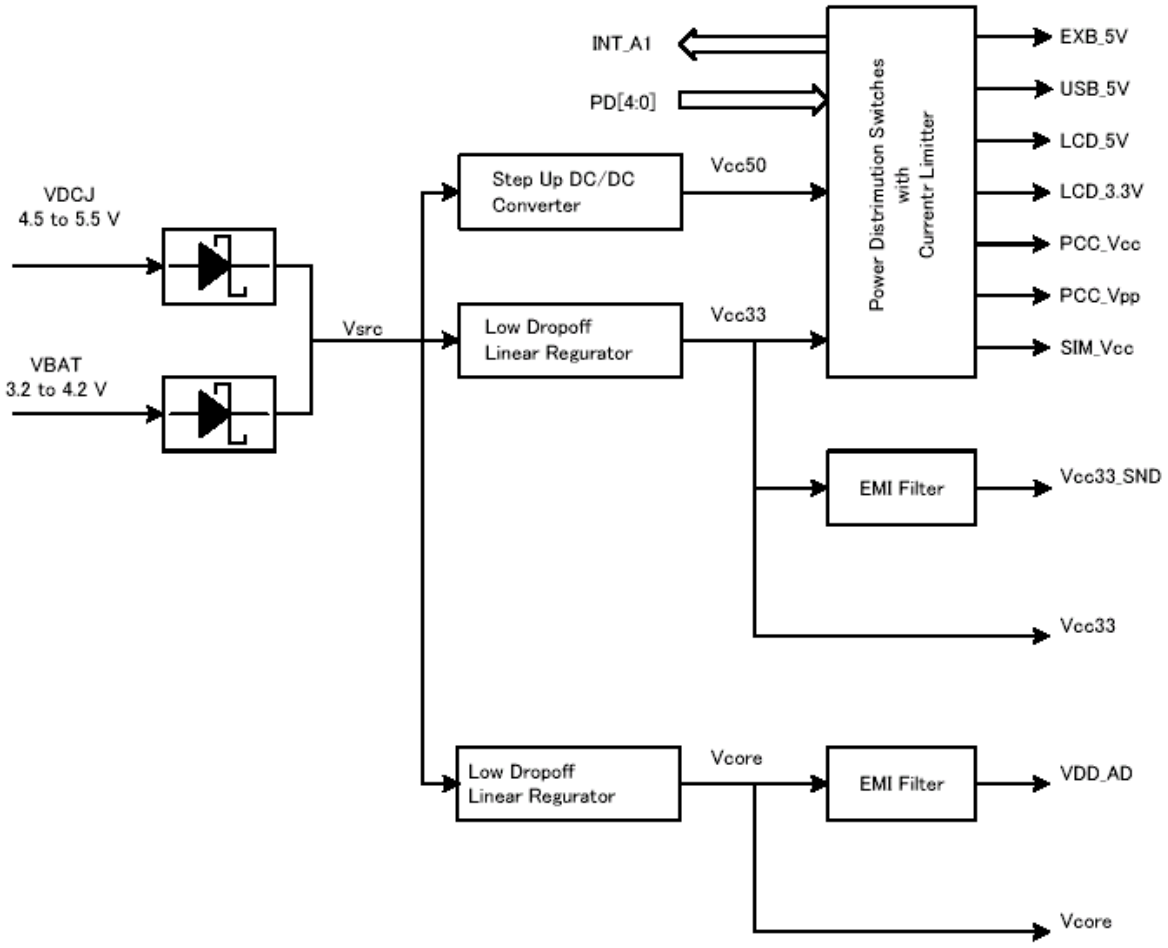


Figure 4.10.2: Example of power supply block structure
(from ARM926 T-Engine)

■ Chapter 5 Power management design for T-Engine hardware

5.1 Power modes (e.g., power save mode)

This section describes implementation methods for each power mode in the T-Engine specifications (i.e., P0, 1, 2, and 3).

Specifications for the P0 mode assume that the main power would be off in this mode. However, since a push type power switch is implemented, power must be connected to the switch to make it operational. For this reason, power is supplied to some circuitry at all times.

Modes P1 and P2 are implemented using software, by setting the MPU to the sleep, doze, stop, or similar states. It is assumed that an MPU with a power management function would be used. In general, power save mode is implemented in one of two ways: by stopping the functioning of the MPU's core only while still running peripheral circuitry or by stopping the MPU's clock and accepting interrupts only. In general, such a state with volatile main memory such as SDRAM not retained is referred to as P1 mode, while such a state with memory retained is referred to as P2 mode.

Mode P3 refers to the state in which the MPU is not set to the sleep, doze, stop, or similar states. Each of modes P1, P2, and P3 assumes changes to the internal state of the MPU only. If no circuitry is added for this purpose, it can be said that there are no differences between these in terms of hardware.

5.2. Power supply controls (power on/off)

Two methods are used for turning the power on: turning the power on with power supply and turning the power on using a power switch. It is possible to use a DIP switch or other means to switch between these methods.

Since T-Engine uses a push type power switch, when controlling the power supply using hardware it is not possible to set power consumption to zero completely. However, the design should enable reducing power consumption to as little as possible.

There are two methods of controlling power supply: implementing hardware logic circuits and via software switches using MPU interrupts. However, when using the latter method the MPU would be set to sleep, doze, stop, or a similar mode when the power is turned off, making it impossible to implement the P0 mode (main power off) covered in the specifications.

The following sections are separated into implementation of hardware and software power control methods.

5.2.1. Hardware power-control design

Figure 5.2.1 shows an example structure for implementation of hardware power control.

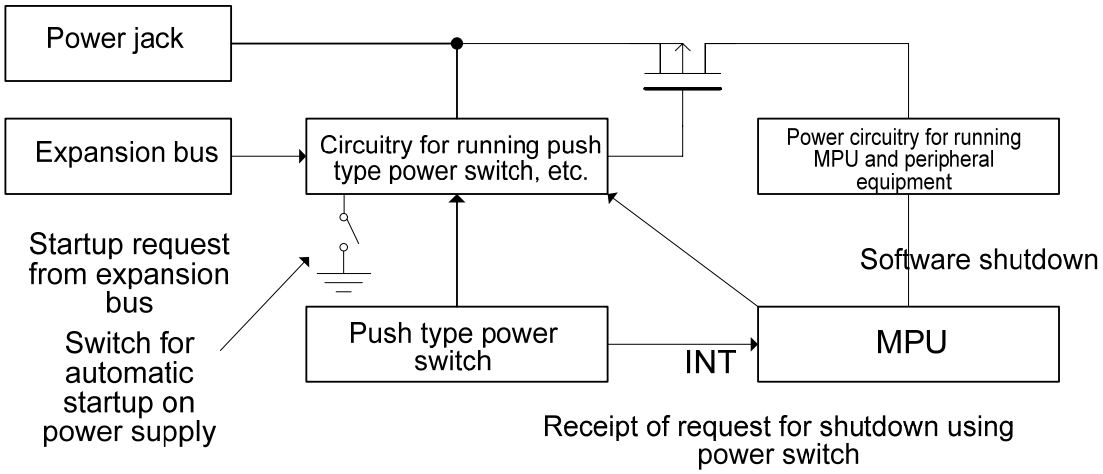


Figure 5.2.1: Configuration example when power supply control is implemented with hardware.

When the push type power switch is depressed, for startup the power is turned on unconditionally. However, for shutdown the MPU is first notified, and then the MPU cuts off the power.

A switch for automatic startup on power supply is implemented to turn on the power unconditionally when a power supply is attached.

5.2.2. Software power-control design

Figure 5.2.2 shows an example structure for implementation of software power control.

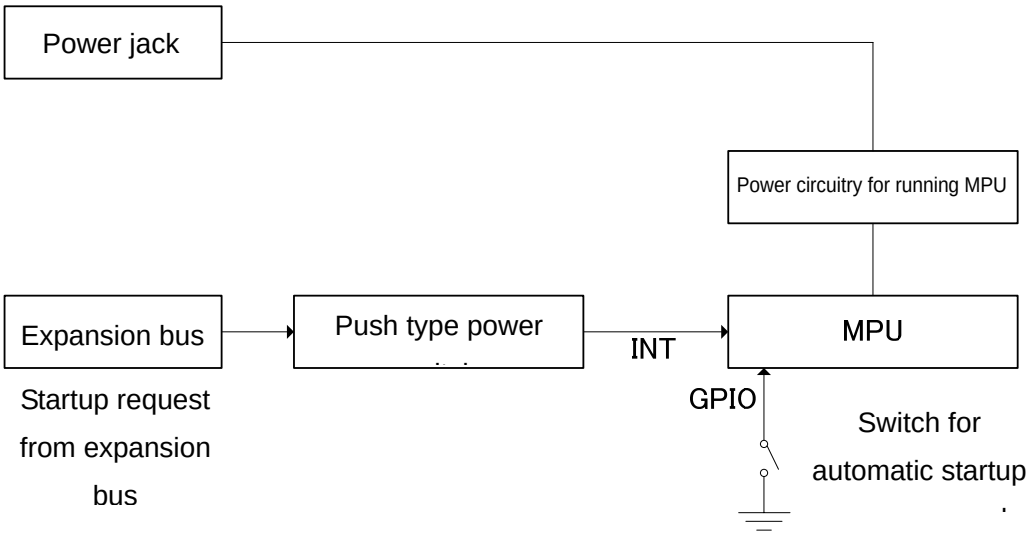


Figure 5.2.2: Configuration example when power supply control is implemented with software.

When implementing software power control, a register for determining the cause of a reset, which would not be affected by resetting the MPU, is required. If this register is not included on board the MPU, an external register is used.

Figure 5.2.3 shows the startup software sequence when using a register for determining the cause of a reset. (The initial value of the register for determining the cause of a reset is 0.)

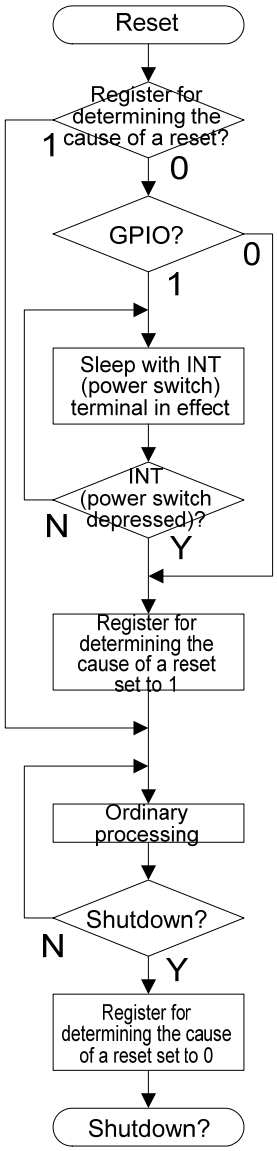


Figure 5.2.3: Startup software sequence

5.3. Linkage with an external expansion board

This section covers points requiring caution when supplying power to an external expansion board through special circuitry for that purpose or when supplying power using the BATT terminal, a specification shared by numerous companies.

Since an external expansion board is connected to the main board using bus wiring, when supplying power or receiving power supply, synchronization with the power supply to the boundary bus buffer and other components must be taken into consideration. Implementation of startup and termination methods in line with the following sample sequence is desirable.

5.3.1 When supplying power to an external expansion board

Figure 5.2.4 shows a sequence diagram for supplying power to an external expansion board on startup.

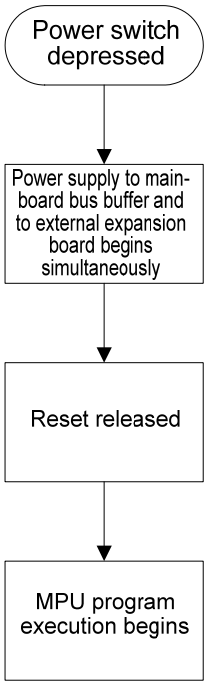


Figure 5.2.4: Sequence diagram for supplying power

The termination sequence is shown in Figure 5.2.5

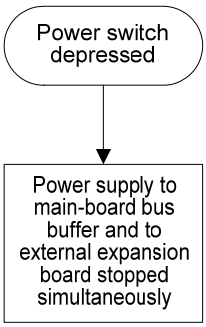


Figure 5.2.5: Termination sequence

It is also acceptable to send notice via signal lines or other means instead of supplying power to the external expansion board directly. Figure 5.2.6 diagram shows the relations between such connections.

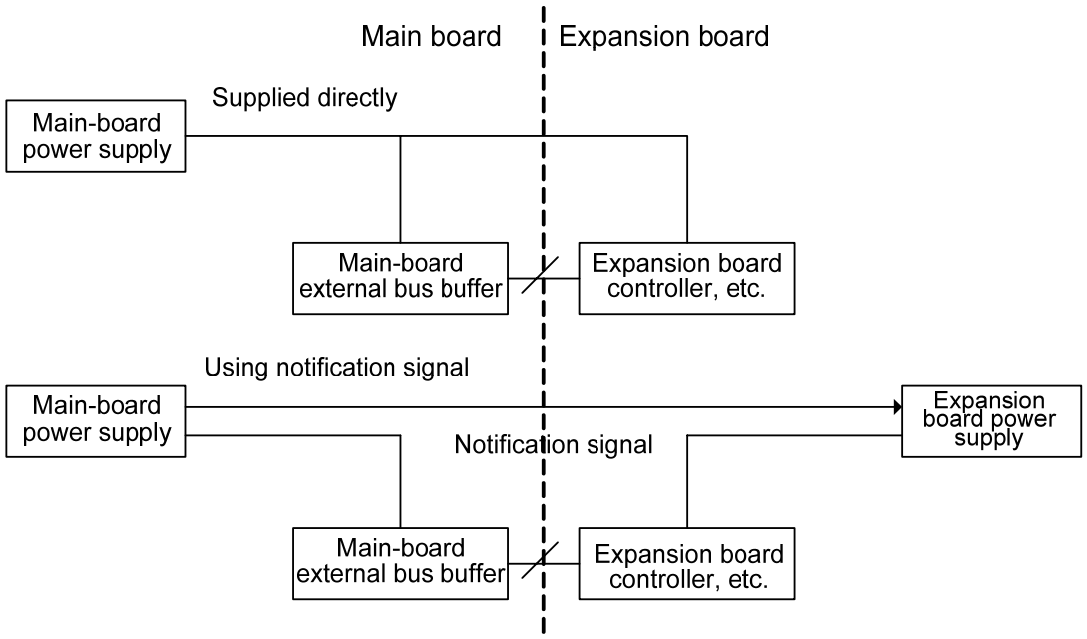


Figure 5.2.6: External expansion board relations between connections

When using a power supply method based on the expansion board, such as wake on LAN, issues related to synchronizing these and bus specifications for connected controller switches need to be taken into consideration.

5.3.2 When receiving power supply from the external expansion board

When supplying power from an external expansion board to the main board using the BATT terminal, a specification shared by numerous companies, power supply to the bus-buffer element connected to the expansion bus must be controlled in a synchronized manner, for example by ensuring that the external expansion board accepts power supply only from the main board or by receiving notification signals.

5.4. Handling power failures

Whether a power failure has occurred can be ascertained by retaining the cause of a reset in a register with a backup power supply, such as an RTC. By manipulating and reading the value in this register, software can ascertain the reason for the current startup. A sequence diagram is shown in Figure 5.4.1.

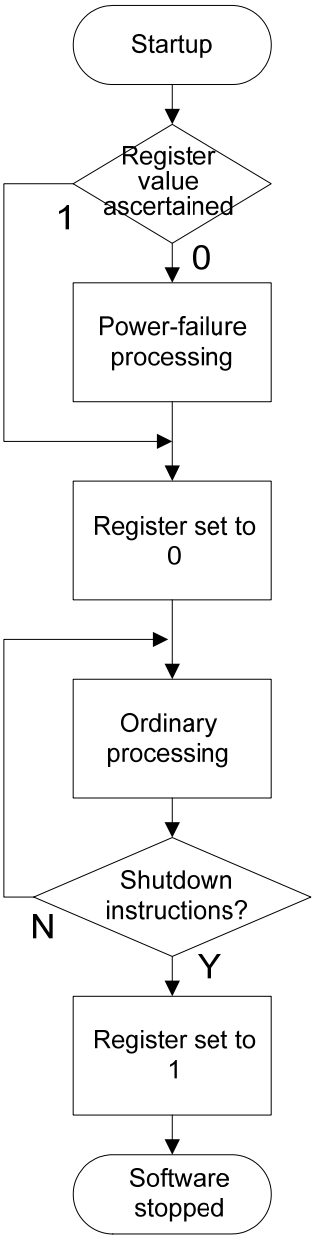


Figure 5.4.1: Power Supply sequence in case of black out.

In addition, it is recommended that the external expansion terminal have a connecting terminal for receiving notice of power failure from UPS equipment and signals for notification of drops in battery voltage, or similar means be taken, to detect power failures when running on backup power.

■ Chapter 6 Actual examples of T-Engine design

This chapter describes overall board structure using as examples T-Engine products that have actually been released. T-Engine devices can be separated into the following two categories based on the signals connected to the boards' expansion bus connectors:

- Local-bus-based T-Engine
- PCI-bus-based T-Engine

A local-bus-based T-Engine is one in which the CPU address bus, data bus, control signals, etc. are connected to the expansion bus connector. A PCI-bus-based T-Engine is one to which a PCI bus is connected as well as a local bus. Table 6.1 shows local-bus-based and PCI-bus-based T-Engine devices currently released.

Table 6.1: Local-bus-based and PCI-bus-based T-Engine boards

	Local-bus-based	PCI-bus-based
Standard T-Engine	SH7727 T-Engine	SH7715R T-Engine
	SH7760 T-Engine	VR5500 T-Engine
	SH7720 T-Engine	VR5701 T-Engine
	SH7780 T-Engine	TX4956 T-Engine
	ARM720-LH7 T-Engine	PPC-V4FX T-Engine
	ARM922-LH7 T-Engine	
	ARM926-MB8 T-Engine	
	ARM920-MX1 T-Engine	
	ARM926-MX21 T-Engine	
μT-Engine	SH7145 μT-Engine	VR4131 uT-Engine
	M32104 μT-Engine	
	M32192 μT-Engine	
	V850E/MA3 μT-Engine	
	Nios Ⅱ μT-Engine	
	ARM-LH79532 μT-Engine	

6.1. Example of local-bus-based T-Engine product design

This section describes the example of a standard T-Engine with the SuperH™-family SH7760 processor on board.

● Structure:

The SH7760 standard T-Engine hardware consists of three boards: the CPU board, an LCD board, and a debugging board. The devices and peripheral interfaces on each board are listed below.

◆ CPU board:

In addition to the following basic standardized structure for a standard T-Engine board, the SH7760 T-Engine board also has its own unique interfaces. Figures 6.1-a and 6.1-b show the board structure.

- SH7760 (SH-4 core)
- Flash memory
- SDRAM
- eTRON SIM card interface
- Real time clock
- PC card interface
- Serial interface
- USB host interface
- Audio input/output interface
- LCD/Touch panel interface
- Expansion bus interface

◆ LCD board:

This LCD board can be connected to any standard T-Engine board. For some companies' products, this is an optional board. It is included in the SH7760 T-Engine development kit.

- TFT color LCD panel
- Touch panel interface
- Push type switch, pointer control
- Infrared remote control receiver module

◆ Debugging board:

The debugging board is an expansion board. Devices and interfaces on this board are not standardized. However, the board's size is standardized.

- EPROM
- Eight-bit LED
- JTAG interface

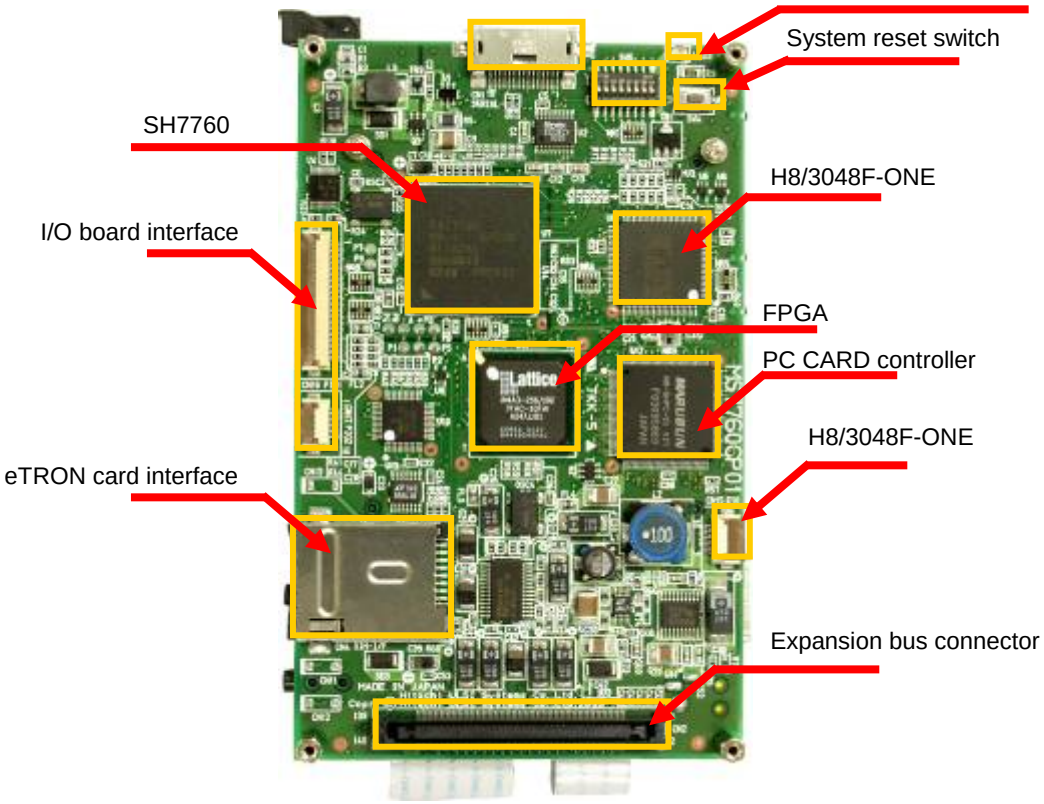


Figure 6.1-a: T-Engine structural diagram (CPU side)

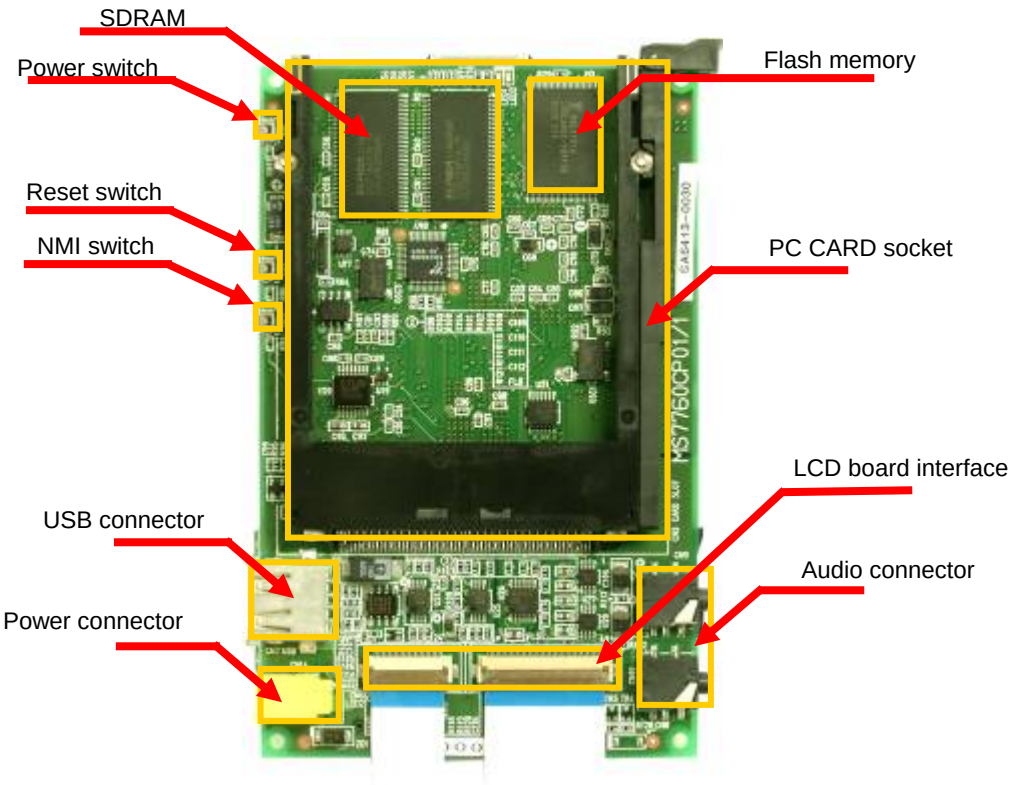


Figure 6.1-b: T-Engine structural diagram (underside)

The following interfaces shown in Figure 6.1-a are additional functions unique to the SH7760 T-Engine:

- I/O board interface
- Infrared remote control transmitting LED

◆ I/O board interface:

This is an additional interface unique to this board and not included in standard T-Engine standards. This connector handles output from the terminals of internal modules on the SH7760. It makes it possible to connect with various external interfaces by connecting the I/O board (expansion board) included with the product. The following internal modules output to this connector:

- Renesas Technology Controller area network 2 (HCAN2): 2ch
- Serial communication interface (SCIF): 2ch
- IIC bus interface: 1ch
- A/D converter: 4ch
- Compare match timer (CMT)

◆ Infrared remote control transmitting LED

This LED is compatible with two types of infrared remote control signal formats (NEC format and Kaseikyo format). It can transmit infrared remote control signals up to 255 bytes.
The receiver for infrared remote control signals is on the LCD board.

Also, this board has a H8/3048F-ONE (H8/300H-series 16-bit single-chip microcomputer) unit on board as a power supply controller. By writing firmware to the flash memory on the H8/3048F-ONE, the following functions can be controlled:

- Real-time clock (RTC)
- System power (3.3 V, 5 V) on/off
- Reading touch panel coordinates
- Key entry
- Sending and receiving infrared remote control signals
- Electronic volume
- Reading/writing serial EEPROM

Table 6.2 shows an overview of SH7760 T-Engine specifications.

Table 6.2: Overview of SH7760 T-Engine specifications

Item		Specifications
CPU		SH7760 (SH-4); implemented operating frequency: 200 MHz
	Cache	16 KB (instruction) + 32 KB (data)
	MMU	Y
	Debugger	JTAG interface
RAM		64 MB
ROM		8 MB
Interface functions	eTRON SIM card interface	Y
	Serial interface	16,550 compatible (max.: 115,200 bps)
	Real time clock	Y
	Audio I/O interface	Headset: 1ch; headphone output: 1ch
	USB host interface	Y (USB1.1 compatible)
	PC card interface	Y (Type 2, one slot)
	LCD/Touch panel interface	Y
	DIP switch	Two (16 bit)
Expansion bus		Local bus (32 bit) Expansion bus connector type: 01-01
Board size		75 mm x 120 mm
Other functions	Infrared input port	Receiver on LCD board
	LED	One (eight bit)

● Block diagram

Figure 6.3 shows a SH7760 T-Engine block diagram.
As shown in Figure 6.3, the SH7760 is connected to peripheral devices via an 8-/16-/32-bit local bus.

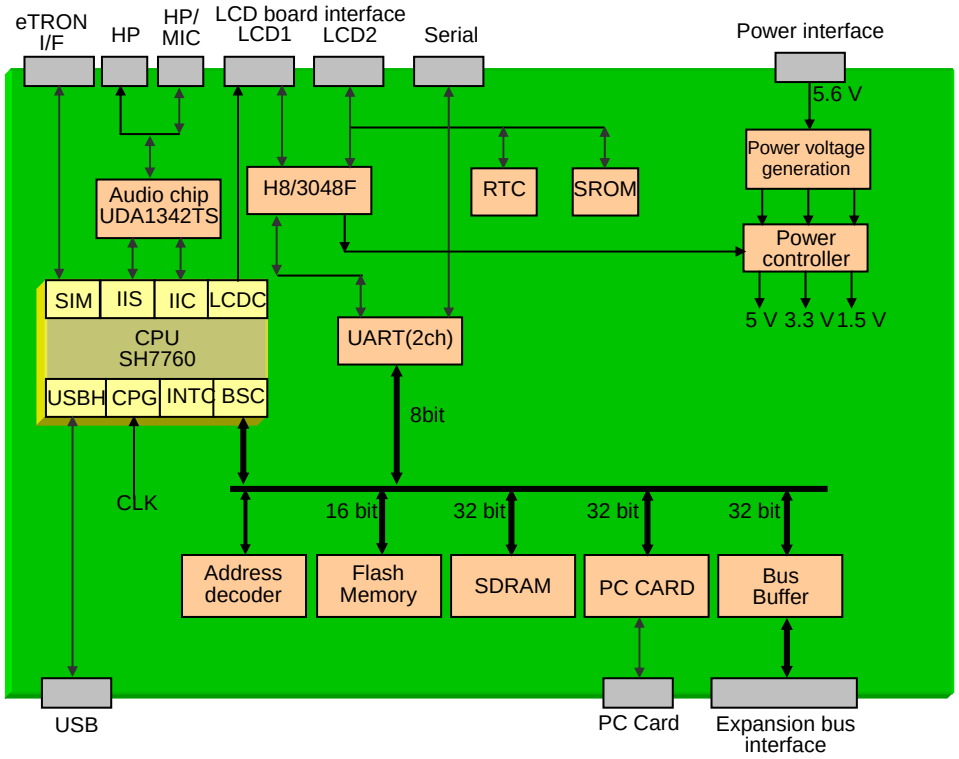


Figure 6.2: SH7760 T-Engine block diagram

SH7760 has many built-in peripheral controllers. Therefore, various interfaces can be realized with the built-in controllers. Or they can be realized by using sub-control microcomputer (H8/3048F-ONE) that is installed as power supply controller.

- Serial interface:
  Uses an NS16C550 compatible UART serial controller and an RS-232C interface driver.

- PC card interface:
  Uses a controller compatible with 68-pin card slots compliant with the PC Card Standard 97.

- LCD/Touch panel interface:
  Outputs signals from the SH7760's on-board LCD controller. The interface with the touch panel on the LCD board is implemented via the H8/3048F-ONE.

- eTRON SIM card interface:
  Uses the smart card interface (SIM) controller on board the SH7760.

- USB host interface:
  Uses the USB host controller (USB 1.1 compliant) on board the SH7760.

- Audio input/output interface:
  Uses the serial Audio interface (SSI) on board the SH7760. Has an Audio CODEC on board. Audio can be output to headphones connected to the mini jack for audio output and can be input from and output to a headset connected to the mini jack for audio input and output.

- Expansion bus interface:
  The address bus, the data bus (32 bits), control signals, and a power supply are output to this interface. The address bus, the data bus, and the control signals are connected via the bus buffer. Table 6.3 shows the pin arrangement for the expansion bus.

- Power interface:
  Power is supplied via an AC adapter (5.6 V/3.5 A). The SH7760 T-Engine uses the following voltages:
  3.3 V: Power supply for on-board logic circuitry
  1.5 V: SH7760 core voltage
  5.0 V: Voltage supplied to PC cards, USB devices, etc.

Table 6.3: Expansion bus connector pin arrangements

Pin No.	Signal	I/O	Pin No.	Signal	I/O	Pin No.	Signal	I/O	Pin No.	Signal	I/O
1	5V (*1)	-	36	D29	I/O	71	A24	OUT	106	SCIF2_CTS#	IN
2	5V	-	37	D30	I/O	72	A25	OUT	107	―	―
3	5V	-	38	D31	I/O	73	EPROMCE#	OUT	108	―	―
4	5V	-	39	GND	-	74	CS2#	OUT	109	GND	-
5	D0	I/O	40	GND	-	75	CS4#	OUT	110	GND	-
6	D1	I/O	41	CKIO	OUT	76	CS5#	OUT	111	TCK	IN
7	D2	I/O	42	GND	-	77	RDWR	OUT	112	TMS	IN
8	D3	I/O	43	GND	-	78	BS#	OUT	113	TRST#	IN
9	D4	I/O	44	GND	-	79	GND	-	114	TDI	IN
10	D5	I/O	45	A0	OUT	80	GND	-	115	TDO	OUT
11	D6	I/O	46	A1	OUT	81	RD#	OUT	116	ASEBRKAK#	OUT
12	D7	I/O	47	A2	OUT	82	WAIT#	IN	117	3.3VSB (*3)	-
13	D8	I/O	48	A3	OUT	83	WE0#	OUT	118	3.3VSB	-
14	D9	I/O	49	A4	OUT	84	WE1#	OUT	119	3.3VSB	-
15	D10	I/O	50	A5	OUT	85	WE2#	OUT	120	3.3VSB	-
16	D11	I/O	51	A6	OUT	86	WE3#	OUT	121	AUDATA0	I/O
17	D12	I/O	52	A7	OUT	87	GND	-	122	AUDATA1	I/O
18	D13	I/O	53	A8	OUT	88	GND	-	123	AUDATA2	I/O
19	D14	I/O	54	A9	OUT	89	IRQ0#	IN	124	AUDATA3	I/O
20	D15	I/O	55	A10	OUT	90	IRQ1#	IN	125	AUDSYNC#	OUT
21	GND	-	56	A11	OUT	91	IRQ2#	IN	126	AUDCK	IN
22	GND	-	57	A12	OUT	92	IRQ3#	IN	127	3.3V (*4)	―
23	D16	I/O	58	A13	OUT	93	NMI_IN	IN	128	3.3V	―
24	D17	I/O	59	A14	OUT	94	RST_IN#	IN	129	3.3V	―
25	D18	I/O	60	A15	OUT	95	RST_OUT#	OUT	130	3.3V	―
26	D19	I/O	61	GND	-	96	DREQ#	IN	131	3.3V	―
27	D20	I/O	62	GND	-	97	DRAK#	OUT	132	3.3V	―
28	D21	I/O	63	A16	OUT	98	DACK#	OUT	133	VBAT_IN (*5)	―
29	D22	I/O	64	A17	OUT	99	ROMSEL	IN	134	VBAT_IN	―
30	D23	I/O	65	A18	OUT	100	BASE# (*2)	IN	135	VBAT_IN	-
31	D24	I/O	66	A19	OUT	101	GND	-	136	VBAT_IN	-
32	D25	I/O	67	A20	OUT	102	GND	-	137	GND	-
33	D26	I/O	68	A21	OUT	103	SCIF2_TXD	OUT	138	GND	-
34	D27	I/O	69	A22	OUT	104	SCIF2_RXD	IN	139	GND	-
35	D28	I/O	70	A23	OUT	105	SCIF2_RTS#	OUT	140	GND	-

Shaded areas ▭ denote SH7760 address bus, data bus, control signals, and serial signals. The electrical power level is 3.3 V.

*1: When the SH7760 unit's power is on, power of 5.0 V (typ.) is supplied.

*2: By setting this terminal to the low level, the SH7760 expansion bus will be output to the expansion bus connector.

*3: When a battery or an AC adapter is connected, power of 3.3 V (typ.) is supplied at all times.

*4: When the SH7760 unit's power is on, power of 3.3 V (typ.) is supplied.

*5: This is the terminal for the power supply (3.6 - 4.2 V). Power can be supplied to the T-Engine board via the expansion bus connector.

● Memory map:

Table 6.4 shows the memory map when the CPU board is used alone.

CS0 area: This is the area for flash memory and EPROM. When the CPU board is run alone, only flash memory is used. When a debugging board is connected, both flash memory and EPROM can be used. When using a debugging board, the arrangements of flash memory and EPROM may be switched. Switching is done by using the DIP switch on the debugging board. When not using a debugging board, these flash memory/EPROM switch settings are ignored.

CS1 area: This is the board control register area.

CS2 area: This area is for use by the expansion slot exclusively. When this area is accessed, the expansion bus's CS2# signal is asserted.

CS3 area: This is the SDRAM area.

CS4 area: This area is for use by the expansion slot exclusively. When this area is accessed, the expansion bus's CS4# signal is asserted.

CS5 area: This area is for use by the expansion slot exclusively. When this area is accessed, the expansion bus's CS5# signal is asserted.

CS6 area: This area is for use in connecting the following peripheral devices:
(1) PC card controller
(2) UART
(3) ID register

CS7 area: This is a reserved area.

Table 6.4: Memory map

Area No.	Bus width	Space	Space name	Device	Notes
CS0 area	16 bit	h'00000000 to h'00FFFFFF	Flash memory area	8 MB MBM29DL640E-90TN (Fujitsu) x 1	
		h'01000000 to h'03FFFFFF	—	Unused area	
CS1 area	16 bit	h'04000000 to h' 07FFFFFF	Board control register area	16 MB Board control register	
CS2 area	8/16/32 bit	h'08000000 to h'0BFFFFFF	Expansion area (CS2)	64MB Expansion slot (CS2 area)	Expansion slot CS2# assertion
CS3 area	32 bit	h'0C000000 to h'0FFFFFFF	SDRAM area	64 MB EDS2516APTA-75 (ELPIDA) x2	
CS4 area	8/16/32 bit	h'10000000 to h'13FFFFFF	Expansion area (CS4)	64 MB Expansion slot (CS4 area)	Expansion slot CS4# assertion
CS5 area	8/16/32 bit	h'14000000 to h'17FFFFFF	Expansion area (CS5)	64 MB Expansion slot (CS5 area)	Expansion slot CS5# assertion
CS6 area	16 bit	h'18000000 to h'19FFFFFF	PC CARD area	Card controller Model: MR-SHPC-01 V2T (Marubun)	
		h'1A000000 to h'1A7FFFFF	UART area (ChA)	UART Model: ST16C2550CQ48 (EXAR) (Referred to as "UART" hereinafter)	Used as interface with H8/3048F-ONE
		h'1A800000 to h'1AFFFFFF	UART area (ChB)	Same as above	Used for host serial interface
		h'1B000000 to h'1BFFFFFF	ID register area		Reads DIP switch settings
CS7 area	—	h'1C000000 to h'1FFFFFFF	—	—	Reserved

6.2. Example of PCI-bus-based T-Engine product design

This section describes the example of a standard T-Engine with the SuperH-family SH7751R processor on board.

● Structure:

The SH7751R standard T-Engine hardware consists of three boards: the CPU board, an LCD board, and a debugging board.

The devices and peripheral interfaces on each board are listed below.

◆ CPU board:

In addition to the following basic standardized structure for a standard T-Engine board, the SH7751R T-Engine board also has its own unique interfaces.

- SH7751R (SH-4 core)
- Flash memory
- SDRAM
- eTRON SIM card interface
- Real time clock
- PC card interface
- Serial interface
- USB host interface
- Audio input/output interface
- LCD/Touch panel interface
- Expansion bus interface

◆ LCD board:

This LCD board can be connected to any standard T-Engine board. For some companies' products, this is an optional board. It is included in the SH7751R T-Engine development kit.

- TFT color LCD panel
- Tablet interface
- Push type switch, pointer control
- Infrared remote control receiver module

◆ Debugging board:

The debugging board is an expansion board. Devices and interfaces on this board are not standardized. However, the board's size is standardized.

- EPROM
- Eight-bit LED
- JTAG interface

The following interface is an additional function unique to the SH7751R T-Engine:

◆ Infrared remote control transmitting LED

This LED is compatible with two types of infrared remote control signal formats (NEC format and Kaseikyo format). It can transmit infrared remote control signals up to 255 bytes.
The receiver for infrared remote control signals is on the LCD board.

Also, this board has a H8/3048F-ONE (H8/300H-series 16-bit single-chip microcomputer) unit on board as a power supply controller. By writing firmware to the flash memory on board the H8/3048F-ONE, the following functions can be controlled:

- Real-time clock (RTC)
- System power (3.3 V, 5 V) on/off
- Reading touch panel coordinates
- Key entry
- Sending and receiving infrared remote control signals
- Electronic volume
- Reading/writing serial EEPROM

- Functional blocks

  Table 6.5 shows an overview of SH7751R T-Engine specifications. Figure 6.4 shows a block diagram.
  As shown in Figure 6.4, the SH7751R is connected to peripheral devices via an 8-/16-/32-bit SH local bus and a PCI bus.

- Serial interface:
  Uses an NS16C550 compatible UART serial controller and an RS-232C interface driver.

- PC card interface:
  Uses a controller compatible with 68-pin card slots compliant with the PC Card Standard 97.

- LCD/Touch panel interface:
  The LCD controller has display memory (10Mbit SDRAM) on board and is capable of displaying 16-bit RGB data in QVGA size. The interface with the touch panel on the LCD board is implemented via the H8/3048F-ONE.

- eTRON SIM card interface:
  Uses the smart card interface (SIM) controller on board the SH7751R.

- USB host interface:
  Uses a USB host controller (USB 2.0 compliant) that can be connected to a PCI bus.

- Audio input/output interface:
  Uses the serial IO controller (SIOF). Has an A/D, D/A converter for use with digital audio. Audio can be output to headphones connected to the mini jack for audio output and can be input from and output to a headset connected to the mini jack for audio input and output.

- Expansion bus interface:
  The local bus (16 bits), the PCI bus, control signals, and a power supply are output to this interface.
  The PCI bus controller (PCIC) built in to the SH7751R is used. The PCIC is compatible with the PCI Ver. 2.1 standard and has a bus width of 32 bits and an operating frequency of 33 MHz.
  Table 6.6 shows the pin arrangement for the expansion bus connector.

- Power interface:
  Power is supplied via an AC adapter (5.6 V/3.5 A). The SH7751R T-Engine uses the following internal voltages:

  3.3 V: Power supply for on-board logic circuitry
  5 V: SH7751R core voltage
  5.0 V: Voltage supplied to PC cards, USB devices, etc.

Table 6.5: Overview of SH7751R T-Engine specifications

Item		Specifications
CPU		SH7751R (SH-4); implemented operating frequency: 240 MHz
	Cache	16 KB (instruction) + 32 KB (data)
	MMU	Y
	Debugger	JTAG interface
RAM		64 MB
ROM		8 MB
Interface functions	eTRON I/F	Y
	Serial I/F	16,550 compatible (max.: 115,200 bps)
	Calendar/clock	Y
	Audio I/F	Headset: 1ch; headphone output: 1ch
	USB host I/F	Y (USB1.1 compatible)
	PC CARD I/F	Y (Type 2, one slot)
	Touch panel I/F	Y
	LCD panel I/F	Y
	DIP switch	Two (16 bit)
	LED	One (eight bit)
Expansion bus		PCI bus/local bus Expansion bus connector type: 04-01
Board size		75 mm x 120 mm
Other functions	Infrared input port	Receiver on LCD board

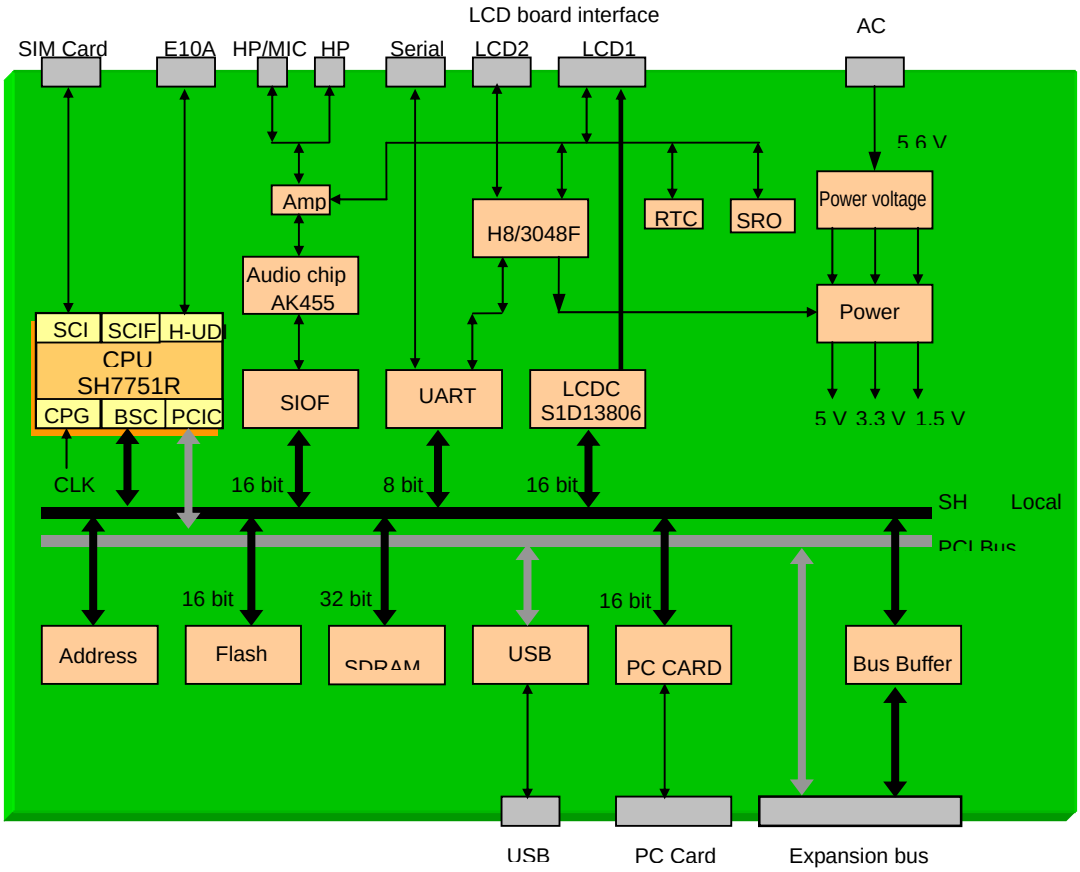


Figure 6.3: Block diagram

Table 6.6: Expansion bus connector pin arrangement

Pin No.	Signal	I/O	Pin No.	Signal	I/O	Pin No.	Signal	I/O	Pin No.	Signal	I/O
1	GND	-	36	AD20	I/O	71	AD2	I/O	106	A1	OUT
2	PCLK2	OUT	37	GND	-	72	AD3	I/O	107	A8	OUT
3	GND	-	38	AD18	I/O	73	GND	-	108	A0	OUT
4	PCLK1	OUT	39	GND	-	74	AD1	I/O	109	RESV	-
5	GND	-	40	AD17	I/O	75	GND	-	110	WR#	OUT
6	PCLK0	OUT	41	CBE3#	I/O	76	AD0	I/O	111	GND	-
7	REQ2#	IN	42	AD16	I/O	77	PCIRST#	OUT	112	RD#	OUT
8	VCCIO	-	43	CBE2#	I/O	78	LOBAT	-	113	D15	I/O
9	REQ1#	IN	44	STOP#	I/O	79	MPOWER	OUT	114	D7	I/O
10	VCCIO	-	45	LOCK#	I/O	80	INTA#	IN	115	D14	I/O
11	REQ0#	IN	46	PERR#	I/O	81	WAKEUP	IN	116	D6	I/O
12	GNT2#	OUT	47	IRDY#	I/O	82	INTB#	IN	117	D13	I/O
13	GND	-	48	TRDY#	I/O	83	INT1#	IN	118	D5	I/O
14	GNT1#	OUT	49	GND	-	84	INTC#	IN	119	D12	I/O
15	GND	-	50	FRAME#	I/O	85	INT2#	IN	120	D4	I/O
16	GNT0#	OUT	51	GND	-	86	INT0#	IN	121	D11	I/O
17	AD31	I/O	52	DEVSEL#	I/O	87	A17	OUT	122	D3	I/O
18	IDSEL2	OUT	53	PAR	I/O	88	CS1#	OUT	123	D10	I/O
19	AD30	I/O	54	SERR#	I/O	89	A16	OUT	124	D2	I/O
20	IDSEL1	OUT	55	CBE1#	I/O	90	CS0#	OUT	125	D9	I/O
21	AD29	I/O	56	AD15	I/O	91	A15	OUT	126	D1	I/O
22	IDSEL0	OUT	57	CBE0#	I/O	92	IORDY	IN	127	D8	I/O
23	AD27	I/O	58	AD14	I/O	93	GND	-	128	D0	I/O
24	AD28	I/O	59	AD12	I/O	94	A7	OUT	129	VBAT	-
25	GND	-	60	AD13	I/O	95	A14	OUT	130	VBAT	-
26	AD26	I/O	61	GND	-	96	A6	OUT	131	VBAT	-
27	GND	-	62	AD11	I/O	97	A13	OUT	132	VBAT	-
28	AD25	I/O	63	GND	-	98	A5	OUT	133	VBAT	-
29	AD23	I/O	64	AD10	I/O	99	A12	OUT	134	VBAT	-
30	AD24	I/O	65	AD8	I/O	100	A4	OUT	135	VBAT	-
31	AD22	I/O	66	AD9	I/O	101	A11	OUT	136	VBAT	-
32	CS2#	OUT	67	AD6	I/O	102	A3	OUT	137	GND	-
33	AD21	I/O	68	AD7	I/O	103	A10	OUT	138	GND	-
34	EPCE#	OUT	69	AD4	I/O	104	A2	OUT	139	GND	-
35	AD19	I/O	70	AD5	I/O	105	A9	OUT	140	BRD_IN#	-

Blue	PCI bus
Green	Local bus
Orange	Power Control
Reverse	Power

● Memory map:

Table 6.7 shows the memory map when the CPU board is used alone.

CS0 area: This is the area for flash memory and EPROM. When the CPU board is run alone, only flash memory can be used. When a debugging board is connected, both flash memory and EPROM can be used.
When using a debugging board, the arrangements of flash memory and EPROM may be switched. Switching is done by using the DIP switch on the debugging board. When not using a debugging board, these flash memory/EPROM switch settings are ignored.

CS1 area: This area is for use by the expansion slot exclusively. When this area is accessed, the expansion bus's CS0# signal is asserted.

CS2 area: This area is used for connecting the LCD controller.

CS3 area: This is the SDRAM area.

CS4 area: This area is for use by the expansion slot exclusively. When this area is accessed, the expansion bus's CS1# signal is asserted.

CS5 area: This area is for use by the expansion slot exclusively. When this area is accessed, the expansion bus's CS2# signal is asserted.

CS6 area: This area is for use in connecting the following peripheral devices:
(1) PC card controller
(2) UART
(3) CODEC interface/board control FPGA

CS7 area: This area is exclusively for PCI memory, register, and I/O use.

Table 6.7: Memory map

Area No.	Bus width	Space	Space name	Device	Notes
CSO area	16 bit	h'00000000 to h'007FFFFF	Flash memory area	8 MB MBM29DL640E90TN (Fujitsu x 1) x 1	
		h'00800000 to h'00FFFFFF	—	Flash memory area image	
		h'01000000 to h'03FFFFFF	—	Unused area	
CS1 area	16 bit	h'04000000 to h'0407FFFF	Expansion area (CS0)	512 KB Expansion slot (CS0) area	Expansion slot CS0# assertion
		h'04080000 to h'07FFFFFF	—	Expansion area (CS0) image	
CS2 area	16 bit	h'08000000 to h'083FFFFF	LCD controller area	LCD controller Model: S1D13806F00A (EPSON)	Referred to as "LCDC" hereinafter
		h'08400000 to h'0BFFFFFF	—	LCD controller area image	
CS3 area	32 bit	h'0C000000 to h'0FFFFFFF	SDRAM area	64MB EDS2516APTA-60 (ELPIDA) x 2	
CS4 area	16 bit	h'10000000 to h'1007FFFF	Expansion area (CS1)	512 KB Expansion slot (CS1) area	Expansion slot CS1# assertion
		h'10080000 to h'13FFFFFF	—	Expansion area (CS1) image	
CS5 area	16 bit	h'14000000 to h'1407FFFF	Expansion area (CS2)	512 KB Expansion slot (CS2) area	Expansion slot CS2# assertion
		h'14080000 to h'17FFFFFF	—	Expansion area (CS2) image	
CS6 area	16 bit	h'18000000 to h'19FFFFFF	PC card area	Card controller Model: MR-SHPC-01 V2T (Marubun)	
		h'1A000000 to h'1A00000F	UART area (ChA)	UART Model: ST16C2550CQ48 (EXAR)	Referred to as "UART" hereinafter
		h'1A000010 to h'1A7FFFFF	—	UART area (ChA) image	
		h'1A800000 to h'1A80000F	UART area (ChB)	Same as above	
		h'1A800010 to h'1AFFFFFF	—	UART area (ChB) image	
		h'1B000000 to	FPGA register area	FPGA register area for control of SIOF and other boards	

		h’1B0000FF			
		h’1B000100 to h’1B7FFFFF	—	FPGA register area image	
		h’1B800000 to h’1BFFFFFF	—	Unused area	
		h’FC000000 to h’FCFFFFFF			
CS7 area		h’FD000000 to h’FDFFFFFF	PCI memory area		
		h’FE000000 to h’FE1FFFFF			
		h’FE200000 to h’FE23FFFF	PCI register area		
		h’FE200000 to h’FE23FFFF	PCI I/O area		
		h’FE240000 to h’FFFFFFFF			

6.3. Conclusion

Table 6.8 features the content of Table 6.1 (categorization of local-bus- and PCI-bus-based T-Engine boards) with the key nos. of connectors used on each board added.

Sorting by key no. shows that local-bus-based T-Engine expansion bus connector pin arrangements come in five types while PCI-bus-based T-Engine expansion bus connector pin arrangements are standardized.

Designing expansion bus connector pin arrangements to match the key nos. of existing T-Engine products makes it possible to reuse expansion boards with different devices and eliminates the need to build a connector with a new key no., among other benefits. As a result, such design can lead to shortened development periods and reduced development costs.

When designing a board, compliance with T-Engine standards is required. Also, giving consideration to expansion bus connector pin arrangement is recommended.

Table 6.8: T-Engine categories by expansion bus connector keying

	Local-bus-based	Key No.	PCI-bus-based	Key No.
Standard T-Engine	SH7727 T-Engine	01-01	SH7715R T-Engine	04-01
	SH7760 T-Engine	01-01	VR5500 T-Engine	04-04
	ARM720-LH7 T-Engine	03-03	VR5701 T-Engine	04-04
	ARM922-LH7 T-Engine	03-03	TX4956 T-Engine	04-04
	ARM926-MB8 T-Engine	03-03	PPC-V4FX T-Engine	04-04
	ARM920-MX1 T-Engine	03-03	-	-
	ARM926-MX21 T-Engine	03-03	-	-
µT-Engine	SH7145 µT-Engine	01-02	VR4131 µT-Engine	04-04
	M32104 µT-Engine	02-02	-	-
	M32192 µT-Engine	02-02	-	-
	V850/MA3 µT-Engine	01-02	-	-
	Nios Ⅱ µT-Engine	06-06	-	-
	ARM-LH79532 µT-Engine	03-03	-	-

Appendix A:

Table A1: Standard T-Engine and µT-Engine boards developed or under development (as of February 2006)

Model	CPU architecture	Expansion bus connector keying	Other notes
T-Engine/SH7727	SH3-DSP(RENESAS)	01-01	With LCD board
T-Engine/SH7751R	SH-4 (RENESAS)	04-01	With LCD board
T-Engine/SH7760	SH-4 (RENESAS)	01-01	With LCD board
T-Engine/SH7720	SH3-DSP (RENESAS)	01-01	With LCD board
T-Engine/SH7780	SH-4A (RENESAS)	04-01	With LCD board
T-Engine/VR5500	MIPS (NEC)	04-04	With RGB output
T-Engine/VR5701	MIPS (NEC)	04-04	With RGB output With IDE I/F
T-Engine/TX4956	MIPS (TOSHIBA)	04-04	With RGB output
T-Engine/ARM720-S1C	ARM7 (EPSON)	03-03	
T-Engine/ARM920-MX1	ARM9 (Freescale)	03-03	
T-Engine/ARM720-LH7	ARM7 (NXP)	03-03	
T-Engine/ARM922-LH7	ARM9 (NXP)	03-03	
T-Engine/ARM926-MB8	ARM9 (FUJITSU)	03-03	With ETM connector
T-Engine/ARM926-MX21	ARM9 (Freescale)	03-03	
T-Engine/PPC-V4FX	PowerPC (XILIX)	04-04	With LAN board
µT-Engine/SH7145	SH-2 (RENESAS)	01-02	
µT-Engine/M32104	M32R (RENESAS)	02-02	With LAN board, With AR board
µT-Engine/M32192	M32R (RENESAS)	02-02	With LAN board, With AR board
µT-Engine/VR4131	MIPS (NEC)	04-04	CPU features MMU
µT-Engine/V850E-MA3	V850 (NEC)	01-02	
µT-Engine/ARM7-LH79532	ARM7 (NXP)	03-03	
µT-Engine/Nios II	Nios II (ALTERA)	06-06	

T-Engine Design Guideline (Ver.1.00.01)

TEF010-S007-01.00.01/en

June 2009

About this specification, please refer to follows;

T-Engine Forum

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Pin	V850E/MA3 uT-Engine			SH7145 uT-Engine			SH7727 T-Engine			SH7760 T-Engine		
Key	01-02			01-02			01-01			01-01		
No.	Signal	I/O	Comment	SH7145	I/O	Comment	SH7727	I/O	Comment	SH7760	I/O	Comment
1	ANo0	OUT	D/A output ch0	NC	-		+5V	OUT	5V output when CPU power is ON	+5V	OUT	5V output when CPU power is ON
2	ANo1	OUT	D/A output ch1	NC	-		+5V	OUT		+5V	OUT	
3	MODE0	IN	MODE signal from ROM writer	NC	-		+5V	OUT		+5V	OUT	
4	MODE1	IN		NC	-		+5V	OUT		+5V	OUT	
5	AD0	I/O	Connect via dumping resistor 22Ω.	D0	I/O	Direct connection to CPU	D0	I/O	Connected via bus buffer	D0	I/O	Connected via bus buffer
6	AD1	I/O		D1	I/O		D1	I/O		D1	I/O	
7	AD2	I/O		D2	I/O		D2	I/O		D2	I/O	
8	AD3	I/O		D3	I/O		D3	I/O		D3	I/O	
9	AD4	I/O		D4	I/O		D4	I/O		D4	I/O	
10	AD5	I/O		D5	I/O		D5	I/O		D5	I/O	
11	AD6	I/O		D6	I/O		D6	I/O		D6	I/O	
12	AD7	I/O		D7	I/O		D7	I/O		D7	I/O	
13	AD8	I/O		D8	I/O		D8	I/O		D8	I/O	
14	AD9	I/O		D9	I/O		D9	I/O		D9	I/O	
15	AD10	I/O		D10	I/O		D10	I/O		D10	I/O	
16	AD11	I/O		D11	I/O		D11	I/O		D11	I/O	
17	AD12	I/O		D12	I/O		D12	I/O		D12	I/O	
18	AD13	I/O		D13	I/O		D13	I/O		D13	I/O	
19	AD14	I/O		D14	I/O		D14	I/O		D14	I/O	
20	AD15	I/O		D15	I/O		D15	I/O		D15	I/O	
21	GND	-		GND	GND		GND	GND		GND	GND	
22	GND	-		GND	GND		GND	GND		GND	GND	
23	P10	I/O		PD16	OUT		D16	I/O	Connected via bus buffer	D16	I/O	Connected via bus buffer
24	P11	I/O		PD17	OUT		D17	I/O		D17	I/O	
25	P12	I/O		PD18	OUT		D18	I/O		D18	I/O	
26	P13	I/O		PD19	OUT		D19	I/O		D19	I/O	
27	+2.5VSB	-	Used by ROM writer	NC	-		D20	I/O		D20	I/O	
28	P14	I/O		PD21	I/O		D21	I/O		D21	I/O	
29	N.C.	-		CONT1	OUT		D22	I/O		D22	I/O	
30	N.C.	-		COND2	OUT		D23	I/O		D23	I/O	
31	DMARQ0	IN		_DREQ0	IN		D24	I/O		D24	I/O	
32	P15	I/O		PD25	I/O		D25	I/O		D25	I/O	
33	DMAAK0	OUT		DACK0	OUT		D26	I/O		D26	I/O	
34	PCM2	I/O		PD27	I/O		D27	I/O		D27	I/O	
35	PCM3	I/O		PD28	OUT		D28	I/O		D28	I/O	
36	PBD1	I/O		PD29	OUT		D29	I/O		D29	I/O	
37	PBD2	I/O		PD30	OUT		D30	I/O		D30	I/O	
38	PCT6	I/O		PD31	OUT		D31	I/O		D31	I/O	
39	GND	-		GND	GND		GND	GND		GND	GND	
40	GND	-		GND	GND		GND	GND		GND	GND	
41	BUSCLK	OUT		CK	OUT		CKIO	OUT		CKIO	OUT	
42	GND	-		GND	GND		GND	GND		GND	GND	
43	GND	-		GND	GND		GND	GND		GND	GND	
44	GND	-		GND	GND		GND	GND		GND	GND	
45	A0	OUT	Connect via dumping resistor 22Ω.	A0	OUT	Direct connection to CPU	A0	OUT	Connected via bus buffer	A0	OUT	Connected via bus buffer
46	A1	OUT		A1	OUT		A1	OUT		A1	OUT	
47	A2	OUT		A2	OUT		A2	OUT		A2	OUT	
48	A3	OUT		A3	OUT		A3	OUT		A3	OUT	
49	A4	OUT		A4	OUT		A4	OUT		A4	OUT	
50	A5	OUT		A5	OUT		A5	OUT		A5	OUT	
51	A6	OUT		A6	OUT		A6	OUT		A6	OUT	
52	A7	OUT		A7	OUT		A7	OUT		A7	OUT	
53	A8	OUT		A8	OUT		A8	OUT		A8	OUT	
54	A9	OUT		A9	OUT		A9	OUT		A9	OUT	
55	A10	OUT		A10	OUT		A10	OUT		A10	OUT	
56	A11	OUT		A11	OUT		A11	OUT		A11	OUT	
57	A12	OUT		A12	OUT		A12	OUT		A12	OUT	
58	A13	OUT		A13	OUT		A13	OUT		A13	OUT	
59	A14	OUT		A14	OUT		A14	OUT		A14	OUT	
60	A15	OUT		A15	OUT		A15	OUT		A15	OUT	
61	GND	-		GND	GND		GND	GND		GND	GND	
62	GND	-		GND	GND		GND	GND		GND	GND	
63	A16	OUT	Connect via dumping resistor 22Ω.	A16	OUT		A16	OUT	Connected via bus buffer	A16	OUT	Connected via bus buffer
64	A17	OUT		A17	OUT		A17	OUT		A17	OUT	
65	A18	OUT		A18	OUT		A18	OUT		A18	OUT	
66	A19	OUT		A19	OUT		A19	OUT		A19	OUT	
67	A20	OUT		A20	OUT		A20	OUT		A20	OUT	
68	A21	OUT		A21	OUT		A21	OUT		A21	OUT	
69	A22	OUT		NC	-		A22	OUT		A22	OUT	
70	A23	OUT		NC	-		A23	OUT		A23	OUT	
71	A24	OUT	Connect via dumping resistor 22Ω.	NC	-		A24	OUT		A24	OUT	
72	A25	OUT		NC	-		A25	OUT		A25	OUT	
73	Pull-Up	-	Unused (Pull-Up)	_EPROMCE	OUT		_EPROMCE	OUT		_EPROMCE	OUT	
74	CS3-	OUT	Controller on the extended board	_CS3	OUT		_CS2	OUT		_CS2	OUT	
75	CS0-	OUT	Flash ROM on the extended board	NC	-		_CS4	OUT		_CS4	OUT	
76	EXTTXD1-	OUT	DSUB9pin on the extended board	PE13/TIOC4B	OUT		_CS5	OUT		_CS5	OUT	
77	EXTRXD1-	IN	Directly connected to the connector.	PE13/TIOC4C	OUT		PDWR	OUT		PDWR	OUT	
78	EXTRTS1-	OUT		PE13/TIOC4D	OUT		_BS	OUT		_BS	OUT	
79	GND	-		GND	GND		GND	GND		GND	GND	
80	GND	-		GND	GND		GND	GND		GND	GND	
81	RD-	OUT		_RD	OUT		_RD	OUT		_RD	OUT	
82	WAIT-	IN		_WAIT	IN		_WAIT	IN		_WAIT	IN	
83	LWR-	OUT		_WRL	OUT		_WE0	OUT		_WE0	OUT	
84	UWR-	OUT		_WRL	OUT		_WE1	OUT		_WE1	OUT	
85	So0	OUT	Connected to ROM writer's DataIn	NC	-		_WE2	OUT		_WE2	OUT	
86	Si0.	IN	Connected to ROM writer's DataOut	NC	-		_WE3	OUT		_WE3	OUT	
87	GND	-		GND	GND		GND	GND		GND	GND	
88	GND	-		GND	GND		GND	GND		GND	GND	
89	ANi0	IN	A/D input ch0	NC	-		_IRQ0	IN	Interrupt input	_IRQ0	IN	Interrupt input
90	ANi1	IN	A/D input ch1	NC	-		_IRQ1	IN	Interrupt input	_IRQ1	IN	Interrupt input
91	AGND	-	Analog GND	NC	-		_IRQ2	IN	Interrupt input	_IRQ2	IN	Interrupt input
92	IRQ-	IN	Interrupt input	_IRQ3	IN	Interrupt input	_IRQ3	IN	Interrupt input	_IRQ3	IN	Interrupt input
93	NMIIN	IN	NMI input	NMI_IN	IN	NMI input	NMI_IN	IN	NMI input	NMI_IN	IN	NMI input
94	RES_IN-	IN	RESET input	_RES_IN	IN	RESET input	_RST_IN	IN	RESET input	_RST_IN	IN	RESET input
95	RES_OUT-	OUT	RESET output	_RES_OUT	OUT	RESET output	_RES_OUT	OUT	RESET output	_RES_OUT	OUT	RESET output
96	AGND	-	Analog GND	NC	-		_DREQ0	IN		_DREQ0	IN	
97	ANi2	IN	A/D input ch2	NC	-		_DRAK0	OUT		_DRAK0	OUT	
98	ANi3	IN	A/D input ch3	NC	-		_DACK0	OUT		_DACK0	OUT	
99	Pull-Up	-	Unused (Pull-Up)	_ROMSEL	IN		_ROMSEL	IN		_ROMSEL	IN	
100	ANi4	IN	A/D input ch4	NC	-		_BASE	IN	Extended bus output in Low	_BASE	IN	Extended bus output in Low
101	GND	-		GND	GND		GND	GND		GND	GND	
102	GND	-		GND	GND		GND	GND		GND	GND	
103	TXD3	OUT		SCI_TXD3	OUT		TXD2	OUT		TXD2	OUT	
104	RXD3	IN		SCI_RXD3	IN		RXD2	IN		RXD2	IN	
105	ANi5	IN	A/D input ch5	NC	-		RTS2	OUT		RTS2	OUT	
106	ANi6	IN	A/D input ch6	NC	-		CTS2	IN		CTS2	IN	
107	ANi7	IN	A/D input ch7	NC	-		NC	-		NC	-	
108	SCK0	OUT	Connected to ROM writer's CLK	DBGMD	IN	E10A emulator	ASEMD0	IN	E10A emulator	NC	-	
109	GND	-		GND	GND		GND	GND		GND	GND	
110	GND	-		GND	GND		GND	GND		GND	GND	
111	Pull-Up	-	Unused (Pull-Up)	TCK	IN	E10A emulator	TCK	IN	E10A emulator	TCK	IN	E10A emulator
112	Pull-Up	-	Unused (Pull-Up)	TMS	IN	E10A emulator	TMS	OUT	E10A emulator	TMS	OUT	E10A emulator
113	Pull-Down	-	Unused (Pull-Down)	_TRST	IN		_TRST	OUT	E10A emulator	_TRST	OUT	E10A emulator
114	Pull-Up	-	Unused (Pull-Up)	TDI	IN		TDI	IN	E10A emulator	TDI	IN	E10A emulator
115	Pull-Up	-	Unused (Pull-Up)	TDO	OUT		TDO	OUT	E10A emulator	TDO	OUT	E10A emulator
116	FPCLK	IN	Clock input from ROM	_ASEBRKAK	OUT	E10A emulator	_ASEBRKAK	OUT	E10A emulator	_ASEBRKAK	OUT	E10A emulator
117	+3.3VSB	OUT	Power always ON: +3.3V output	3.3VSB	OUT	Power always ON: +3.3V output	3.3VSB	OUT	Power always ON: +3.3V output	3.3VSB	OUT	Power always ON: +3.3V output
118	+3.3VSB	OUT		3.3VSB	OUT		3.3VSB	OUT		3.3VSB	OUT	
119	+3.3VSB	OUT		3.3VSB	OUT		3.3VSB	OUT		3.3VSB	OUT	
120	+3.3VSB	OUT		3.3VSB	OUT		3.3VSB	OUT		3.3VSB	OUT	
121	CS5-	OUT	Tip select for LCD	PE0/TIOCOA	OUT		AUDATA0	I/O	E10A emulator	AUDATA0	I/O	E10A emulator
122	EXTCTS1-	IN	Same as pins 76-78 above	PE1/TIOCOB	OUT		AUDATA1	I/O	E10A emulator	AUDATA1	I/O	E10A emulator
123	N.C.	-		PE2/TIOCOC	OUT		AUDATA2	I/O	E10A emulator	AUDATA2	I/O	E10A emulator
124	N.C.	-		PE3/TIOCOD	OUT		AUDATA3	I/O	E10A emulator	AUDATA3	I/O	E10A emulator
125	FPRES-	IN	Reset input from ROM writer	PE6/TIOC2A	OUT		_AUDSYNC	IN	E10A emulator	_AUDSYNC	IN	E10A emulator
126	ADTRG	IN	A/D TRIG input	NC	-		AUDCK	OUT	E10A emulator	AUDCK	OUT	E10A emulator
127	+3.3V	OUT	Normal power: +3.3V output	3.3V	OUT	Normal power: +3.3V output	3.3V	OUT	Normal power: +3.3V output	3.3V	OUT	Normal power: +3.3V output
128	+3.3V	OUT		3.3V	OUT		3.3V	OUT		3.3V	OUT	
129	+3.3V	OUT		3.3V	OUT		3.3V	OUT		3.3V	OUT	
130	+3.3V	OUT		3.3V	OUT		3.3V	OUT		3.3V	OUT	
131	+3.3V	OUT		3.3V	OUT		3.3V	OUT		3.3V	OUT	
132	+3.3V	OUT		3.3V	OUT		3.3V	OUT		3.3V	OUT	
133	VBAT-IN	IN	VBAT power input (4.8V-5.6V)	VBAT_IN	IN	VBAT power input (4.8V-5.6V)	VBAT_IN	IN	VBAT power input (4.8V-5.6V)	VBAT_IN	IN	VBAT power input (4.8V-5.6V)
134	VBAT-IN	IN		VBAT_IN	IN		VBAT_IN	IN		VBAT_IN	IN	
135	VBAT-IN	IN		VBAT_IN	IN		VBAT_IN	IN		VBAT_IN	IN	
136	VBAT-IN	IN		VBAT_IN	IN		VBAT_IN	IN		VBAT_IN	IN	
137	GND	-		GND	GND		GND	GND		GND	GND	
138	GND	-		GND	GND		GND	GND		GND	GND	
139	GND	-		GND	GND		GND	GND		GND	GND	
140	GND	-		GND	GND		GND	GND		GND	GND	
	quipped with diode in two places: VBAT_IN and J			Equipped with diode in two places: VBAT_IN and JA			※There is no diode.					

Pin	M32104 µT-Engine			M32192 µT-Engine			VR5500 T-Engine			VR4131 µT-Engine		
Key	02-02			02-02			04-04			04-04		
No.	M32104	I/O	Comment	M32192	I/O	Comment	VR5500	I/O	Comment	VR4131	I/O	Comment
1	GND	GND		GND	GND		GND	GND		GND	GND	
2	GND	GND		GND	GND		PCLK2	OUT		PCLK2	OUT	
3	GND	GND		GND	GND		GND	GND		GND	GND	
4	GND	GND		GND	GND		PCLK1	OUT		PCLK1	OUT	
5	V33	OUT	3.3V power output	V33	OUT	3.3V power output	GND	GND		GND	GND	
6	V33	OUT		V33	OUT		PCLK0	OUT		PCLK0	OUT	
7	V33	OUT		V33	OUT		REQ2#	IN		REQ2#	IN	
8	V33	OUT		V33	OUT		VCCIO	OUT		VCCIO	OUT	
9	JTAG_RST#	IN	For connecting SDI emulator	JTAG_RST#	IN	For connecting SDI emulator	REQ1#	IN		REQ1#	IN	
10	TRST#	IN		TRST#	IN		VCCIO	OUT		VCCIO	OUT	
11	TMS	IN		TMS	IN		REQ0#	IN		REQ0#	IN	
12	TDO	OUT		TDO	OUT		GNT2#	OUT		GNT2#	OUT	
13	TDI	IN		TDI	IN		GND	GND		GND	GND	
14	TCK	IN		TCK	IN		GNT1#	OUT		GNT1#	OUT	
15	GND	GND		GND	GND		GND	IN		GND	IN	
16	GND	GND		GND	GND		GNT0#	OUT		GNT0#	OUT	
17	P77	I/O		P83	I/O		AD31	I/O		AD31	I/O	
18	P76	I/O		P85	I/O		IDSEL2	OUT		IDSEL2	OUT	
19	NC	—		NC	—		AD30	I/O		AD30	I/O	
20	NC	—		NC	—		IDSEL1	OUT		IDSEL1	OUT	
21	P67	I/O		P93	I/O		AD29	I/O		AD29	I/O	
22	P66	I/O		P82	I/O		IDSEL0	OUT		IDSEL0	OUT	
23	P65	I/O		P84	I/O		AD27	I/O		AD27	I/O	
24	P64	I/O		P86	I/O		AD28	I/O		AD28	I/O	
25	P63	I/O		P94	I/O		GND	GND		GND	GND	
26	P62	I/O		P87	I/O		AD26	I/O		AD26	I/O	
27	GND	GND		GND	GND		GND	GND		GND	GND	
28	GND	GND		GND	GND		AD25	I/O		AD25	I/O	
29	P27	I/O		P95	I/O		AD23	I/O		AD23	I/O	
30	P26	I/O		NC	—		AD24	I/O		AD24	I/O	
31	P25	I/O		NC	—		AD22	I/O		AD22	I/O	
32	P24	I/O		P96	I/O		RESV	-		RESV	-	
33	NC	—	Reserved for EXTPWR (external power)	NC	—	Reserved for EXTPWR (external power)	AD21	I/O		AD21	I/O	
34	NC	—	Reserved for EXTPWR (external power)	NC	—	Reserved for EXTPWR (external power)	RESV	-		RESV	-	
35	NC	—	Reserved for V33SB (standing power)	NC	—	Reserved for V33SB (standing power)	AD19	I/O		AD19	I/O	
36	NC	—	Reserved for V33SB (standing power)	NC	—	Reserved for V33SB (standing power)	AD20	I/O		AD20	I/O	
37	GND	GND		GND	GND		GND	GND		GND	GND	
38	GND	GND		GND	GND		AD18	I/O		AD18	I/O	
39	NC	—	Reserved for INT3#	TIN27	IN		GND	GND		GND	GND	
40	NC	—	Reserved for INT2#	TIN18	IN		AD17	I/O		AD17	I/O	
41	NC	—		NC	—		CBE3#	I/O		CBE3#	I/O	
42	NC	—		NC	—		AD16	I/O		AD16	I/O	
43	SW2	OUT		SW2	OUT		CBE2#	I/O		CBE2#	I/O	
44	SW1	OUT		SW1	OUT		STOP#	I/O		STOP#	I/O	
45	LED2	OUT		LED2	OUT		LOCK#	I/O		LOCK#	I/O	
46	LED1	OUT		LED1	OUT		PERR#	I/O		PERR#	I/O	
47	GND	GND		GND	GND		IRDY#	I/O		IRDY#	I/O	
48	GND	GND		GND	GND		TRDY#	I/O		TRDY#	I/O	
49	EXREADY#	IN(O/D)		MPU_WAIT#	IN(O/D)		GND	GND		GND	GND	
50	EXINT	IN		TIN24	IN		FRAME#	I/O		FRAME#	I/O	
51	BCS1#	OUT		BUS_CS#	OUT		GND	GND		GND	GND	
52	BWS3#	OUT		NC	—		DEVSEL#	I/O		DEVSEL#	I/O	
53	BWS2#	OUT		NC	—		PAR	I/O		PAR	I/O	
54	BWS1#	OUT		BUS_BLW#	OUT		SERR#	IN(o/d)		SERR#	IN(o/d)	
55	BWS0#	OUT		BUS_BHW#	OUT		CBE1#	I/O		CBE1#	I/O	
56	BRS#	OUT		BUS_RD#	OUT		AD15	I/O		AD15	I/O	
57	GND	GND		GND	GND		CBE0#	I/O		CBE0#	I/O	
58	GND	GND		GND	GND		AD14	I/O		AD14	I/O	
59	GND	GND		GND	GND		AD12	I/O		AD12	I/O	
60	EXCLK	OUT		BCLK	OUT		AD13	I/O		AD13	I/O	
61	GND	GND		GND	GND		GND	GND		GND	GND	
62	GND	GND		GND	GND		AD11	I/O		AD11	I/O	
63	RESET#	OUT		RESET#	OUT		GND	GND		GND	GND	
64	GND	GND		GND	GND		AD10	I/O		AD10	I/O	
65	GND	GND		GND	GND		AD8	I/O		AD8	I/O	
66	BA30	OUT	Connected via bus buffer	BA30	OUT	Connected via bus buffer	AD9	I/O		AD9	I/O	
67	BA29	OUT		BA29	OUT		AD6	I/O		AD6	I/O	
68	BA28	OUT		BA28	OUT		AD7	I/O		AD7	I/O	
69	BA27	OUT		BA27	OUT		AD4	I/O		AD4	I/O	
70	BA26	OUT		BA26	OUT		AD5	I/O		AD5	I/O	
71	BA25	OUT		BA25	OUT		AD2	I/O		AD2	I/O	
72	BA24	OUT		BA24	OUT		AD3	I/O		AD3	I/O	
73	GND	GND		GND	GND		GND	GND		GND	GND	
74	GND	GND		GND	GND		AD1	I/O		AD1	I/O	
75	BA23	OUT	Connected via bus buffer	BA23	OUT	Connected via bus buffer	GND	GND		GND	GND	
76	BA22	OUT		BA22	OUT		AD0	I/O		AD0	I/O	
77	BA21	OUT		BA21	OUT		PCIRST#	OUT		PCIRST#	OUT	
78	BA20	OUT		BA20	OUT		LOBAT#	IN(o/d)		LOBAT#	IN(o/d)	
79	BA19	OUT		BA19	OUT		MPOWER	OUT		MPOWER	OUT	
80	BA18	OUT		BA18	OUT		INTA#	IN(o/d)		INTA#	IN(o/d)	
81	BA17	OUT		BA17	OUT		WAKEUP#	IN(o/d)		WAKEUP#	IN(o/d)	
82	BA16	OUT		BA16	OUT		INTB#	IN(o/d)		INTB#	IN(o/d)	
83	GND	GND		GND	GND		RESV	-		RESV	-	
84	GND	GND		GND	GND		INTC#	IN(o/d)		INTC#	IN(o/d)	
85	BA15	OUT	Connected via bus buffer	BA15	OUT	Connected via bus buffer	RESV	-		RESV	-	
86	BA14	OUT		BA14	OUT		INT0#	IN(o/d)		INT0#	IN(o/d)	
87	BA13	OUT		BA13	OUT		A17	OUT		A17	OUT	
88	BA12	OUT		BA12	OUT		CS1#	OUT		CS1#	OUT	
89	BA11	OUT		BA11	OUT		A16	OUT		A16	OUT	
90	BA10	OUT		BA10	OUT		CS0#	OUT		CS0#	OUT	
91	BA9	OUT		BA9	OUT		A15	OUT		A15	OUT	
92	BA8	OUT		BA8	OUT	Output fixed to "L"	IORDY#	IN(o/d)		IORDY#	IN(o/d)	
93	GND	GND		GND	GND		GND	GND		GND	GND	
94	GND	GND		GND	GND		A7	OUT		A7	OUT	
95	BD31	I/O	Connected via bus buffer	NC	—		A14	OUT		A14	OUT	
96	BD30	I/O		NC	—		A6	OUT		A6	OUT	
97	BD29	I/O		NC	—		A13	OUT		A13	OUT	
98	BD28	I/O		NC	—		A5	OUT		A5	OUT	
99	BD27	I/O		NC	—		A12	OUT		A12	OUT	
100	BD26	I/O		NC	—		A4	OUT		A4	OUT	
101	BD25	I/O		NC	—		A11	OUT		A11	OUT	
102	BD24	I/O		NC	—		A3	OUT		A3	OUT	
103	GND	GND		GND	GND		A10	OUT		A10	OUT	
104	GND	GND		GND	GND		A2	OUT		A2	OUT	
105	BD23	I/O	Connected via bus buffer	NC	—		A9	OUT		A9	OUT	
106	BD22	I/O		NC	—		A1	OUT		A1	OUT	
107	BD21	I/O		NC	—		A8	OUT		A8	OUT	
108	BD20	I/O		NC	—		RESV	-		RESV	-	
109	BD19	I/O		NC	—		RESV	-		RESV	-	
110	BD18	I/O		NC	—		WR#	OUT		WR#	OUT	
111	BD17	I/O		NC	—		GND	GND		GND	GND	
112	BD16	I/O		NC	—		RD#	OUT		RD#	OUT	
113	GND	GND		GND	GND		D15	I/O		D15	I/O	
114	GND	GND		GND	GND		D7	I/O		D7	I/O	
115	BD15	I/O	Connected via bus buffer	BD15	I/O	Connected via bus buffer	D14	I/O		D14	I/O	
116	BD14	I/O		BD14	I/O		D6	I/O		D6	I/O	
117	BD13	I/O		BD13	I/O		D13	I/O		D13	I/O	
118	BD12	I/O		BD12	I/O		D5	I/O		D5	I/O	
119	BD11	I/O		BD11	I/O		D12	I/O		D12	I/O	
120	BD10	I/O		BD10	I/O		D4	I/O		D4	I/O	
121	BD9	I/O		BD9	I/O		D11	I/O		D11	I/O	
122	BD8	I/O		BD8	I/O		D3	I/O		D3	I/O	
123	GND	GND		GND	GND		D10	I/O		D10	I/O	
124	GND	GND		GND	GND		D2	I/O		D2	I/O	
125	BD7	I/O	Connected via bus buffer	BD7	I/O	Connected via bus buffer	D9	I/O		D9	I/O	
126	BD6	I/O		BD6	I/O		D1	I/O		D1	I/O	
127	BD5	I/O		BD5	I/O		D8	I/O		D8	I/O	
128	BD4	I/O		BD4	I/O		D0	I/O		D0	I/O	
129	BD3	I/O		BD3	I/O		VBAT	I/O	VBAT power input (4.0V-6.0V)	VBAT	I/O	VBAT power input (4.0V-6.0V)
130	BD2	I/O		BD2	I/O		VBAT	I/O		VBAT	I/O	
131	BD1	I/O		BD1	I/O		VBAT	I/O		VBAT	I/O	
132	BD0	I/O		BD0	I/O		VBAT	I/O		VBAT	I/O	
133	V33	OUT	3.3V power output	V33	OUT	3.3V power output	VBAT	I/O		VBAT	I/O	
134	V33	OUT		V33	OUT		VBAT	I/O		VBAT	I/O	
135	V33	OUT		V33	OUT		VBAT	I/O		VBAT	I/O	
136	V33	OUT		V33	OUT		VBAT	I/O		VBAT	I/O	
137	GND	GND		GND	GND		GND	GND		GND	GND	
138	GND	GND		GND	GND		GND	GND		GND	GND	
139	GND	GND		GND	GND		GND	GND		GND	GND	
140	GND	GND		GND	GND		GND	GND		GND	GND	
	※The number (140-1) is the inverse of the number d			※The number (140-1) is the inverse of the number d					※There is no diode.			※There is no diode.

Pin	Tx4956 T-Engine			SH7751R T-Engine			ARM T-Engine			FR T-Engine Appliance		
Key	04-04			04-01			03-03			01-05		
No.	Tx4956	I/O	Comment	SH7751R	I/O	Comment	ARM	I/O	Comment	FR	I/O	Comment
1	GND	—		GND	GND		EXB_5V	-		EXB_5V	-	
2	PCLK2	OUT		PCLK2	OUT		EXB_5V	-		EXB_5V	-	
3	GND	—		GND	GND		EXB_5V	-		EXB_5V	-	
4	PCLK1	OUT		PCLK1	OUT		EXB_5V	-		EXB_5V	-	
5	GND	—		GND	GND		EXB_5V	-		EXB_5V	-	
6	PCLK0	OUT		PCLK0	OUT		EXB_5V	-		EXB_5V	-	
7	REQ2#	IN		REQ2#	IN		D0	I/O	Connected via bus buffer	D0	I/O	Direct connection to CPU
8	VCCIO	OUT	3.3V output when C	VCCIO	-	3.3V output when CPU po	D1	I/O		D1	I/O	
9	REQ1#	IN		REQ1#	IN		D2	I/O		D2	I/O	
10	VCCIO	OUT	3.3V output when C	VCCIO	-	3.3V output when CPU po	D3	I/O		D3	I/O	
11	REQ0#	IN		REQ0#	IN		D4	I/O		D4	I/O	
12	GNT2#	OUT		GNT2#	OUT		D5	I/O		D5	I/O	
13	GND	—		GND	GND		D6	I/O		D6	I/O	
14	GNT1#	OUT		GNT1#	OUT		D7	I/O		D7	I/O	
15	GND	—		GND	GND		D8	I/O		D8	I/O	
16	GNT0#	OUT		GNT0#	OUT		D9	I/O		D9	I/O	
17	AD31	I/O		AD31	I/O		D10	I/O		D10	I/O	
18	IDSEL2	OUT		IDSEL2	OUT		D11	I/O		D11	I/O	
19	AD30	I/O		AD30	I/O		D12	I/O		D12	I/O	
20	IDSEL1	OUT		IDSEL1	OUT		D13	I/O		D13	I/O	
21	AD29	I/O		AD29	I/O		D14	I/O		D14	I/O	
22	IDSEL0	OUT		IDSEL0	OUT		D15	I/O		D15	I/O	
23	AD27	I/O		AD27	I/O		GND			GND		
24	AD28	I/O		AD28	I/O		GND			GND		
25	GND	—		GND	GND		D16	I/O	Connected via bus buffer	D16	I/O	Direct connection to CPU
26	AD26	I/O		AD26	I/O		D17	I/O		D17	I/O	
27	GND	—		GND	GND		D18	I/O		D18	I/O	
28	AD25	I/O		AD25	I/O		D19	I/O		D19	I/O	
29	AD23	I/O		AD23	I/O		D20	I/O		D20	I/O	
30	AD24	I/O		AD24	I/O		D21	I/O		D21	I/O	
31	AD22	I/O		AD22	I/O		D22	I/O		D22	I/O	
32	RESV	—		CS2#	OUT		D23	I/O		D23	I/O	
33	AD21	I/O		AD21	I/O		D24	I/O		D24	I/O	
34	RESV	—		EPCE#	OUT		D25	I/O		D25	I/O	
35	AD19	I/O		AD19	I/O		D26	I/O		D26	I/O	
36	AD20	I/O		AD20	I/O		D27	I/O		D27	I/O	
37	GND	—		GND	GND		D28	I/O		D28	I/O	
38	AD18	I/O		AD18	I/O		D29	I/O		D29	I/O	
39	GND	—		GND	GND		D30	I/O		D30	I/O	
40	AD17	I/O		AD17	I/O		D31	I/O		D31	I/O	
41	CBE3#	I/O		CBE3#	I/O		GND			GND		
42	AD16	I/O		AD16	I/O		GND			GND		
43	CBE2#	I/O		CBE2#	I/O		A0	OUT	Connected via bus buffer	A0	OUT	Direct connection to CPU
44	STOP#	I/O		STOP#	I/O		A1	OUT		A1	OUT	
45	LOCK#	I/O		LOCK#	I/O		A2	OUT		A2	OUT	
46	PERR#	I/O		PERR#	I/O		A3	OUT		A3	OUT	
47	IRDY#	I/O		IRDY#	I/O		A4	OUT		A4	OUT	
48	TRDY#	I/O		TRDY#	I/O		A5	OUT		A5	OUT	
49	GND	—		GND	GND		A6	OUT		A6	OUT	
50	FRAME#	I/O		FRAME#	I/O		A7	OUT		A7	OUT	
51	GND	—		GND	GND		A8	OUT		A8	OUT	
52	DEVSEL#	I/O		DEVSEL#	I/O		A9	OUT		A9	OUT	
53	PAR	I/O		PAR	I/O		A10	OUT		A10	OUT	
54	SERR#	IN(o/d)		SERR#	I/O		A11	OUT		A11	OUT	
55	CBE1#	I/O		CBE1#	I/O		A12	OUT		A12	OUT	
56	AD15	I/O		AD15	I/O		A13	OUT		A13	OUT	
57	CBE0#	I/O		CBE0#	I/O		A14	OUT		A14	OUT	
58	AD14	I/O		AD14	I/O		A15	OUT		A15	OUT	
59	AD12	I/O		AD12	I/O		GND			GND		
60	AD13	I/O		AD13	I/O		GND			GND		
61	GND	—		GND	GND		A16	OUT	Connected via bus buffer	A16	OUT	Direct connection to CPU
62	AD11	I/O		AD11	I/O		A17	OUT		A17	OUT	
63	GND	—		GND	GND		A18	OUT		A18	OUT	
64	AD10	I/O		AD10	I/O		A19	OUT		A19	OUT	
65	AD8	I/O		AD8	I/O		A20	OUT		A20	OUT	
66	AD9	I/O		AD9	I/O		A21	OUT		A21	OUT	
67	AD6	I/O		AD6	I/O		A22	OUT		A22	OUT	
68	AD7	I/O		AD7	I/O		A23	OUT		A23	OUT	
69	AD4	I/O		AD4	I/O		CS0#	OUT		CS0#	OUT	
70	AD5	I/O		AD5	I/O		CS1#	OUT		CS1#	OUT	
71	AD2	I/O		AD2	I/O		CS2#	OUT		CS2#	OUT	
72	AD3	I/O		AD3	I/O		CS3#	OUT		CS3#	OUT	
73	GND	—		GND	GND		WE0#	OUT		WE1#	OUT	
74	AD1	I/O		AD1	I/O		R/W	OUT		R/W	OUT	
75	GND	—		GND	GND		GND	-		GND	-	
76	AD0	I/O		AD0	I/O		GND	-		GND	-	
77	PCIRST#	OUT		PCIRST#	OUT		CLK	OUT		CLK	OUT	
78	LOBAT#	IN(o/d)		LOBAT#	-		BE2#	OUT	Connected via bus buffer	BE2#	OUT	
79	MPOWER	OUT		MPOWER	OUT		GND	-		GND	-	
80	INTA#	IN(o/d)		INTA#	IN		BE3#	OUT	Connected via bus buffer	BE3#	OUT	
81	WAKEUP#	IN(o/d)		WAKEUP#	IN		OE#	OUT		OE#	OUT	Direct connection to CPU
82	INTB#	IN(o/d)		INTB#	IN		RESERVED			RESERVED		
83	RESV	—		INIT1#	IN		BREQ0#	IN		BREQ#	I	
84	INTC#	IN(o/d)		INTC#	IN		BACK#	OUT		BACK#	OUT	
85	RESV	—		INIT2#	IN		BE0#	OUT	Connected via bus buffer	BE0#	OUT	Direct connection to CPU
86	INT0#	IN(o/d)		INT0#	IN		BE1#	OUT		BE1#	OUT	
87	A17	OUT		A17	OUT		WAIT#	IN		WAIT#	IN	
88	CS1#	OUT		CS1#	OUT		DEOT#	OUT		DEOT#	OUT	
89	A16	OUT		A16	OUT		DREQ0#	IN		DREQ0#	IN	
90	CS0#	OUT		CS0#	OUT		DREQ1#	IN		DREQ1#	IN	
91	A15	OUT		A15	OUT		DACK0#	OUT		DACK0#	OUT	
92	IORDY#	IN(o/d)		IORDY#	IN		DACK1#	OUT		DACK1#	OUT	
93	GND	—		GND	GND		GND	-		GND	-	
94	A7	OUT		A7	OUT		GND	-		GND	-	
95	A14	OUT		A14	OUT		RSV0	-	Reserved (specific to eac	N.C.		
96	A6	OUT		A6	OUT		RSV1	-		FPTOUT0	OUT	
97	A13	OUT		A13	OUT		RSV2	-		N.C.		
98	A5	OUT		A5	OUT		RSV3	-		FPTOUT1	OUT	
99	A12	OUT		A12	OUT		RSV4	-		N.C.		
100	A4	OUT		A4	OUT		RSV5	-		FPTOUT2	OUT	
101	A11	OUT		A11	OUT		RSV6	-		N.C.		
102	A3	OUT		A3	OUT		RSV7	-		N.C.		
103	A10	OUT		A10	OUT		RSV8	-		N.C.		
104	A2	OUT		A2	OUT		RSV9	-		N.C.		
105	A9	OUT		A9	OUT		RSV10	-		N.C.		
106	A1	OUT		A1	OUT		RSV11	-		N.C.		
107	A8	OUT		A8	OUT		GND	-		GND	-	
108	RESV	—		A0	OUT		GND	-		GND	-	
109	RESV	—		RESV	-		RSV12	-	Reserved (specific to eac	N.C.		
110	WR#	OUT		WR#	OUT		RSV13	-		N.C.		
111	GND	—		GND	GND		RSV14	-		FWEX	OUT	
112	RD#	OUT		RD#	OUT		RSV15	-		N.C.		
113	D15	I/O		D15	I/O		RSV16	-		N.C.		
114	D7	I/O		D7	I/O		RSV17	-		N.C.		
115	D14	I/O		D14	I/O		RSV18	-		N.C.		
116	D6	I/O		D6	I/O		RSV19	-		VTref		Directly connected to Vi
117	D13	I/O		D13	I/O		RSV20	-		N.C.		
118	D5	I/O		D5	I/O		BATTERY	I/O	For battery board	BATTERY_	I/O	
119	D12	I/O		D12	I/O		RSV22	-	Reserved (specific to eac	N.C.		
120	D4	I/O		D4	I/O		advice_EMI	IN	Signal for ROM disconn	advice_EMI	IN	
121	D11	I/O		D11	I/O		GND	-		GND	-	
122	D3	I/O		D3	I/O		GND	-		GND	-	
123	D10	I/O		D10	I/O		INT	IN	Interrupt	INT	IN	Interrupt
124	D2	I/O		D2	I/O		WDTOUT	OUT	Specific to each hardwar	nRESETO	OUT	Reset output
125	D9	I/O		D9	I/O		PORST#	OUT	Power on reset	PORST#	OUT	Power on reset
126	D1	I/O		D1	I/O		RTCK	OUT	JTAG RTCK	RTCK	OUT	JTAG RTCK
127	D8	I/O		D8	I/O		RESET#	OUT	Reset	RESET#	OUT	Reset
128	D0	I/O		D0	I/O		TRST#	IN	JTAG TRST	TRST#	IN	JTAG TRST
129	VBAT	I/O	VBAT power input (4.0V-6.0V)	VBAT	IN	VBAT power input (4.0V-6.0V)	TCK	IN	JTAG TCK	TCK	IN	JTAG TCK
130	VBAT	I/O		VBAT	IN		TMS	IN	JTAG TMS	TMS	IN	JTAG TMS
131	VBAT	I/O		VBAT	IN		TDI	IN	JTAG TDI	TDI	IN	JTAG TDI
132	VBAT	I/O		VBAT	IN		TDO	OUT	JTAG TDO	TDO	OUT	JTAG TDO
133	VBAT	I/O		VBAT	IN		VBAT	IN	External power (3.6V-5V)	VBAT	IN	External power (3.6V-5V)
134	VBAT	I/O		VBAT	IN		VBAT	IN		VBAT	IN	
135	VBAT	I/O		VBAT	IN		VBAT	IN		VBAT	IN	
136	VBAT	I/O		VBAT	IN		VBAT	IN		VBAT	IN	
137	GND	—		GND	GND		GND	-		GND	-	
138	GND	—		GND	GND		GND	-		GND	-	
139	GND	—		GND	GND		GND	-		GND	-	
140	GND	—		BRD_IN#		LocalBus output in Low (Mostly Lo	GND	-		GND	-	
			※There is no diode.			※There is no diode.	ipped with diode in two places: VBAT_IN and			ipped with diode in two places: VBAT_IN and		

Pin	FPGA Board			ALTERA T-Engine		
Key	00-00			06-06		
No.	ALTERA	I/O	Comment	ALETRA	I/O	Comment
1	FPGA	I/O		+3.3V		
2	FPGA	I/O		+3.3V		
3	FPGA	I/O		+3.3V		
4	FPGA	I/O		+3.3V		
5	FPGA	I/O		GND		
6	FPGA	I/O		GND		
7	FPGA	I/O		GND		
8	FPGA	I/O		GND		
9	FPGA	I/O		ProtoIO0	I/O	
10	FPGA	I/O		ProtoIO1	I/O	
11	FPGA	I/O		ProtoIO2	I/O	
12	FPGA	I/O		ProtoIO3	I/O	
13	FPGA	I/O		ProtoIO4	I/O	
14	FPGA	I/O		ProtoIO5	I/O	
15	FPGA	I/O		ProtoIO6	I/O	
16	FPGA	I/O		ProtoIO7	I/O	
17	FPGA	I/O		ProtoIO8	I/O	
18	FPGA	I/O		ProtoIO9	I/O	
19	FPGA	I/O		ProtoIO10	I/O	
20	FPGA	I/O		ProtoIO11	I/O	
21	FPGA	I/O		GND		
22	FPGA	I/O		GND		
23	FPGA	I/O		ProtoIO12	I/O	
24	FPGA	I/O		ProtoIO13	I/O	
25	FPGA	I/O		ProtoIO14	I/O	
26	FPGA	I/O		ProtoIO15	I/O	
27	FPGA	I/O		ProtoIO16	I/O	
28	FPGA	I/O		ProtoIO17	I/O	
29	FPGA	I/O		ProtoIO18	I/O	
30	FPGA	I/O		ProtoIO19	I/O	
31	FPGA	I/O		ProtoIO20	I/O	
32	FPGA	I/O		ProtoIO21	I/O	
33	FPGA	I/O		ProtoIO22	I/O	
34	FPGA	I/O		ProtoIO23	I/O	
35	FPGA	I/O		ProtoIO24	I/O	
36	FPGA	I/O		ProtoIO25	I/O	
37	FPGA	I/O		ProtoIO26	I/O	
38	FPGA	I/O		ProtoIO27	I/O	
39	FPGA	I/O		GND		
40	FPGA	I/O		GND		
41	FPGA	I/O		ProtoIO28	I/O	
42	FPGA	I/O		ProtoIO29	I/O	
43	FPGA	I/O		ProtoIO30	I/O	
44	FPGA	I/O		ProtoIO31	I/O	
45	FPGA	I/O		ProtoIO32	I/O	
46	FPGA	I/O		ProtoIO33	I/O	
47	FPGA	I/O		ProtoIO34	I/O	
48	FPGA	I/O		ProtoIO35	I/O	
49	FPGA	I/O		ProtoIO36	I/O	
50	FPGA	I/O		ProtoIO37	I/O	
51	FPGA	I/O		ProtoIO38	I/O	
52	FPGA	I/O		ProtoIO39	I/O	
53	FPGA	I/O		ProtoIO40	I/O	
54	FPGA	I/O		CARDSELn	OUT	
55	FPGA	I/O		USER LED0	OUT	
56	FPGA	I/O		USER LED1	OUT	
57	FPGA	I/O		GND		
58	FPGA	I/O		GND		
59	FPGA	I/O		USER LED2	OUT	
60	FPGA	I/O		USER LED3	OUT	
61	FPGA	I/O		USER LED4	OUT	
62	FPGA	I/O		USER LED5	OUT	
63	FPGA	I/O		USER LED6	OUT	
64	FPGA	I/O		USER LED7	OUT	
65	FPGA	I/O		PBRESETn	IN	
66	FPGA	I/O		USER PBn0	IN	
67	FPGA	I/O		USER PBn1	IN	
68	FPGA	I/O		USER PBn2	IN	
69	FPGA	I/O		USER PBn3	IN	
70	FPGA	I/O		ERTS	IN	
71	FPGA	I/O		ETXD	IN	
72	FPGA	I/O		ECTS	O	
73	FPGA	I/O		ERXD	O	
74	FPGA	I/O		POW0n		
75	FPGA	I/O		GND		
76	FPGA	I/O		GND		
77	FPGA	I/O		MICTOR0	I/O	
78	FPGA	I/O		MICTOR1	I/O	
79	FPGA	I/O		MICTOR2	I/O	
80	FPGA	I/O		MICTOR3	I/O	
81	FPGA	I/O		MICTOR4	I/O	
82	FPGA	I/O		MICTOR5	I/O	
83	FPGA	I/O		MICTOR6	I/O	
84	FPGA	I/O		MICTOR7	I/O	
85	FPGA	I/O		MICTOR8	I/O	
86	FPGA	I/O		MICTOR9	I/O	
87	FPGA	I/O		MICTOR10	I/O	
88	FPGA	I/O		MICTOR11	I/O	
89	FPGA	I/O		MICTOR12	I/O	
90	FPGA	I/O		MICTOR13	I/O	
91	FPGA	I/O		MICTOR14	I/O	
92	FPGA	I/O		MICTOR15	I/O	
93	FPGA	I/O		GND		
94	FPGA	I/O		GND		
95	FPGA	I/O		MICTOR16	I/O	
96	FPGA	I/O		MICTOR17	I/O	
97	FPGA	I/O		MICTOR18	I/O	
98	FPGA	I/O		MICTOR19	I/O	
99	FPGA	I/O		MICTOR20	I/O	
100	FPGA	I/O		MICTOR21	I/O	
101	FPGA	I/O		MICTOR22	I/O	
102	FPGA	I/O		MICTOR23	I/O	
103	FPGA	I/O		MICTOR24	I/O	
104	FPGA	I/O		TR CLK	OUT	
105	FPGA	I/O		MICTOR CLK	OUT	
106	FPGA	I/O		TCK	IN	
107	FPGA	I/O		TMS	IN	
108	FPGA	I/O		POW1#	IN	
109	FPGA	I/O		TDI	IN	
110	FPGA	I/O		TDO	OUT	
111	FPGA	I/O		GND		
112	FPGA	I/O		GND		
113	FPGA	I/O		EOSC	OUT	
114	FPGA	I/O		GND		
115	FPGA	I/O		ECLKIN	OUT	
116	FPGA	I/O		GND		
117	FPGA	I/O		ECLKOUT	IN	
118	FPGA	I/O		GND		
119	FPGA	I/O		GND		
120	FPGA	I/O		GND		
121	FPGA	I/O		GND		
122	FPGA	I/O		CONFDONE	OUT	
123	FPGA	I/O		+3.3V		
124	FPGA	I/O		+3.3V		
125	FPGA	I/O		+3.3V		
126	FPGA	I/O		+3.3V		
127	FPGA	I/O		Vunreg		
128	FPGA	I/O		Vunreg		
129	FPGA	I/O		Vunreg		
130	FPGA	I/O		Vunreg		
131	FPGA	I/O		Vunreg		
132	FPGA	I/O		Vunreg		
133	VBAT_IN	IN	External power (3.6V-5V)	Vunreg		voltage range Input; 6.0-9.0v Output; 6.0v
134	VBAT_IN	IN		Vunreg		
135	VBAT_IN	IN		Vunreg		
136	VBAT_IN	IN		Vunreg		
137	GND	-		GND		
138	GND	-		GND		
139	GND	-		GND		
140	GND	-		GND		
	※Equipped with diode in two places: VBAT_				※There is no diode.	